SAMSUNG

Rev. 1.0, May. 2022

MZWLO1T9HCJR-00B5C
MZWLO3T8HCLS-00B5C
MZWLO7T6HBLA-00B5C
MZWLO15THBLA-00B5C

SAMSUNG SSD PM1743

Specification(PCIe® NVMe™ U.2)

Datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor	Revision No.
0.5	1. Initial release	Mar, 25. 2022	Preliminary	Semi Lee	Inyoung Kim
1.0	1. Initial release	May, 18. 2022	Final	Semi Lee	Ilsu Han

Part Number	Capacity[1)]	LBA Count
MZWLO1T9HCJR-00B5C	1.92TB	3,750,748,848
MZWLO3T8HCLS-00B5C	3.84TB	7,501,476,528
MZWLO7T6HBLA-00B5C	7.68TB	15,002,931,888
MZWLO15THBLA-00B5C	15.36TB	30,001,856,512

FEATURES

- PCI Express® Gen.4 / Gen.5
- Single port x4 lanes
- Enhanced Power-Loss Data Protection
- LDPC ECC
- End-to-End Data Protection
- Support up to 127 I/O Queues
- Support Deallocate (a.k.a. TRIM) Command
- Support PCI Express® AER (Advanced Error Reporting)
- Support 127 vectors for MSI-X
- Support SSD Enhanced S.M.A.R.T. Feature Set
- Hardware based AES-XTS 256-bit Encryption Engine
- RoHS / Halogen-Free Compliant
- Static and Dynamic Wear Leveling
- Support NVMe-MI SMBus

DRIVE CONFIGURATION

· Form Factor	SFF-8639 2.5-inch
· Interface	PCI Express® Gen.4 / Gen.5 x4
· Bytes per Sector	512 Bytes

PERFORMANCE SPECIFICATIONS

(1) Gen.5

· Data Transfer Rate[2] (128KB data size)

- Sequential Read	Up to 12,000 MB/s
- Sequential Write	2TB : Up to 2,500 MB/s
	4/8/16TB : Up to 5,000 MB/s

· Data I/O Speed[2] (4KB data size, Sustained)

- Random Read	2TB : Up to 1500K IOPS
	4/8/16TB : Up to 2000K IOPS
- Random Write	2TB : Up to 110K IOPS
	4/8TB : Up to 180K IOPS
	16TB : Up to 200K IOPS

· Latency (Sustained random workload)

- Read/Write (Typ.)[3]	90/20 us
- Drive Ready Time (Typ.)	Up to 28 sec

· Quality of service[3]

- Read/Write (99%)	90 / 20 us

COMPLIANCE

· PCI Express® Base Specification Rev. 5.0
· NVM Express™ Specification Rev. 1.4

CERTIFICATIONS AND DECLARATIONS

· c-UL-us, CE, TUV-GS, CB, BSMI, KC, VCCI, Morocco, RCM, FCC, IC

PRODUCT ECOLOGICAL COMPLIANCE

· RoHS	meet spec

RELIABILITY SPECIFICATIONS

· Uncorrectable Bit Error Rate	1 sector per 10^{17} bits read
· MTBF	2,000,000 hours
· Power on Cycles (Ambient)	20,000
· Component Design Life	5 years
· Endurance	1DWPD
· TBW (@4KB Random Write)	
- 1.92TB	3.504 PB
- 3.84TB	7.008 PB
- 7.68TB	14.016 PB
- 7.68TB	28.032 PB
· Data Retention	3 months

ENVIRONMENTAL SPECIFICATIONS

· Temperature, Case (T_C)[4)]	
- Operating	0 ~ 70 °C
- Non-operating	-40 ~ 85 °C
· Humidity (Non-operating)	5 ~ 95%
· Shock	1,500 G/ 0.5msec
· Vibration	
- Sinusoidal	20 Gpeak, 20 ~ 2000Hz

POWER REQUIREMENTS

· Supply Voltage / Tolerance	12V±10%

POWER CONSUMPTIONS[5)]

· Read Power	22.5W
· Write Power	24W
· Idle (Typ.)	8W

PHYSICAL DIMENSION

· Width	69.85 ± 0.25mm
· Length	100.20 ± 0.25mm
· Height	15.00 +0.00/-0.50mm
· Weight	Up to 190 g

OPERATING SYSTEMS

- Windows Server 2019 64-bit
- Windows Server 2016 64-bit
- Ubuntu 20.04 (Kernel 5.4)
- Ubuntu 18.10 (Kernel 4.18)
- CentOS 8.2 (Kernel 4.18.0-193)
- CentOS 7.6 (Kernel 3.10.0-957)

NOTE: Specifications are subject to change without notice.

1) 1TB = 10^{12} Bytes, unformatted Capacity.
User accessible capacity may vary depending on operating environment and formatting.
2) Based on PCI Express® Gen5 x4, Random performance measured using FIO in 18.04.2 LTS with queue depth 64 by 16 workers(Jobs) and Sequential performance with queue depth 128 by 1 worker. Actual performance may vary depending on use conditions and environment.
3) The read/write latency and Quality of Service are measured by using FIO in 18.04.2 LTS and 4KB transfer size with queue depth 1 on a random workload of sustained state.
4) Case temperature (Tcase(Tc)) based on the hottest point on the external case surface. Highly recommending sufficient airflow to operate properly on heavier workload within the operating temperature. Performance throttling will be engaged at higher temperature (80°C) over the operating temperature.
5) Typical Power Consumption
(Maximum average power with a measurement period of 500ms.)

Table Of Contents

1.0 INTRODUCTION

1.1 General Description

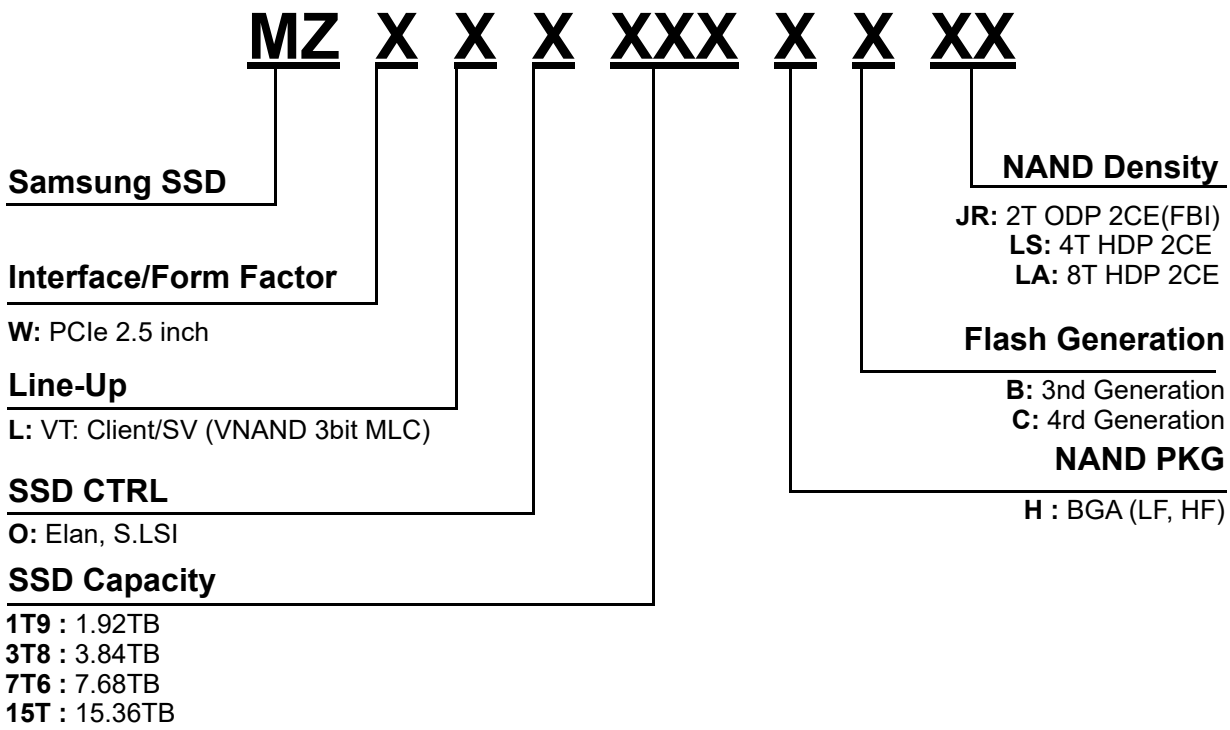
This document describes the specifications of the Samsung SSD PM1743, which is a native-PCIe SSD for enterprise application.
The Samsung SSD PM1743 presents outstanding performance with instant responsiveness to the host system, by applying the Peripheral Component Interconnect Express (PCIe) 5.0 interface standard, as well as highly efficient Non-Volatile Memory Express (NVMe) Protocol.
The Samsung SSD PM1743 delivers wide bandwidth of (12GB/s) for sequential read speed and (5GB/s) for sequential write speed under 25W power.
By combining the enhanced reliability Samsung NAND Flash memory silicon with NAND Flash management technologies, the Samsung SSD PM1743 delivers the extended endurance of up to 1 Drive Writes Per Day (DWPD) for 5 years, which is suitable for enterprise applications, in one 2.5-inch form factor lineup: 1.92TB, 3.84TB, 7.68TB, 15.36TB.
In addition, the Samsung SSD PM1743 supports Hot Plug insertion and removal feature by employing the efficient circuitry for Power Loss Protection (PLP) and handling inrush current. PLP solution can guarantee that data issued by the host system are written to the storage media without any loss in the event of sudden power off or sudden power failure. Inrush current handler can protect the internal components from the electrical and physical damages.

1.2 Product List

[Table 1] Product List

Type	Capacity	Part Number
U.2	1.92TB	MZWLO1T9HCJR-00B5C
	3.84TB	MZWLO3T8HCLS-00B5C
	7.68TB	MZWLO7T6HBLA-00B5C
	15.36TB	MZWLO15THBLA-00B5C

1.3 Ordering Information



2.0 PRODUCT SPECIFICATIONS

2.1 Capacity

[Table 2] User Capacity and Addressable Sectors

Capatity[1) 2)]	LBA Count
1.92TB	3,750,748,848
3.84TB	7,501,476,528
7.68TB	15,002,931,888
15.36TB	30,001,856,512

NOTE:
1) 1TB = 10^{12} Bytes, 1 Sector = 512Bytes
2) Capacity shown in Table 2 represents the total usable capacity of the SSD which may be less than the total physical capacity.
A certain area in physical capacity, not in the area shown to the user, might be used for the purpose of NAND flash management.

2.2 Performance

[Table 3] Sustained Random Read/Write Performance (IOPS)

Maximum Performance[1)]		Unit	1.92TB	3.84TB	7.68TB	15.36TB
PCIe Gen.5	Random 4KB Read	IOPS	1500K	2000K	2000K	2000K
	Random 4KB Write	IOPS	110K	180K	180K	200K

NOTE:
1) Random performance in Table 3 PCIe GEN5 was measured by using FIO in Ubuntu 18.04.2 LTS with queue depth 64 by 16 workers(Jobs).
Actual performance may vary depending on use conditions and environment.

[Table 4] Sequential Read/Write Performance

Maximum Performance[1)]		Unit	1.92TB	3.84TB	7.68TB	15.36TB
PCIe Gen.5	Sequential 128KB Read	MB/s	12,000	12,000	12,000	12,000
	Sequential 128KB Write	MB/s	2,500	5,000	5,000	5,000

NOTE:
1) Sequential performance in Table 4 PCIe GEN5 was measured by using FIO in Ubuntu 18.04.2 LTS with queue depth 64 by 16 worker(Job).
Actual performance may vary depending on use conditions and environment.

2.3 Latency

[Table 5] Latency[1] (sustained state)

Queue Depth = 1		Unit	1.92TB	3.84TB	7.68TB	15.36TB
PCIe Gen.5	4KB Random Read/Write[2)]	us	90 / 20	90 / 20	90 / 20	90 / 20
	Sequential Read/Write[3)]	us	100 / 40	100 / 40	100 / 40	100 / 40
Drive Ready Time[4)]		sec	5	8	14	28

NOTE:
1) Typical values.
2) The random read/write latency is measured by using FIO in Ubuntu 18.04.2 LTS and 4KB transfer size with queue depth 1 on a random workload of sustained state.
3) The sequential read/write latency is measured by using FIO in Ubuntu 18.04.2 LTS and 128KB transfer size with queue depth 1 on a sequential workload of sustained state.
4) The maximum taking time to be ready for receiving commands after power-up (CSTS.Ready=1). It is expected that I/O commands may not be completed at this point.

2.4 Quality of Service (QoS)

[Table 6] Quality of Service (QoS)

Quality of Service (99%)		Unit	1.92TB	3.84TB	7.68TB	15.36TB
PCIe Gen.5	Read(4KB)(QD=1,Job=1)	us	90	90	90	90
	Write(4KB)(QD=1,Job=1)	us	20	20	20	20
	Read(4KB)(QD=64,Job=4)	ms	1	1	1	1
	Write(4KB)(QD=64,job=4)	ms	20	20	20	20

Quality of Service (99.99%)		Unit	1.92TB	3.84TB	7.68TB	15.36TB
PCIe Gen.5	Read(4KB)(QD=1,Job=1)	us	120	120	120	120
	Write(4KB)(QD=1,Job=1)	us	50	50	50	50
	Read(4KB)(QD=64,Job=4)	ms	2	2	2	2
	Write(4KB)(QD=64,Job=4)	ms	40	40	40	40

NOTE:
1) QoS is measured using FIO (99/99.99 %) with queue depth 1, Job=1 on sigle port and queue depth 64, Job=4 for on 4KB random and write.
2) QoS is measured as the maximum round-trip time taken for 99 % of commands to host.
3) QoS is measured as the maximum round-trip time taken for 99.99 % of commands to host.

2.5 IOPS Consistenc

[Table 7] IOPS Consistency

IOPS Consistency[1, 2]	Unit	1.92TB	3.84TB	7.68TB	15.36TB
Random Read (4 KB)	%	95	95	95	95
Random Write (4 KB)	%	90	90	90	90

NOTE:
1) IOPS consistency measured using FIO with queue depth 128, worker 4.
2) IOPS Consistency (%) = (IOPS in the 99.9% slowest 1-second interval)/(average IOPS during the test).

2.6 Power

The Samsung SSD PM1743 is implemented in standardized 2.5-inch form factor and gets primary 12V power as well as auxiliary 3.3V (3.3Vaux) power through the indicated pins (#P13~15 for 12V and #E3 for 3.3Vaux in SFF-8639 connector plug) from the host system.
For 12V and 3.3Vaux, the allowable voltage tolerance and noise level in SSD are described in chapter 2.6.1, the power consumption in chapter 2.6.2.

2.6.1 Operating Voltage(12V and 3.3Vaux)

[Table 8] Operating Voltage Conditions[1)]

Operating Voltage	1.92TB	3.84TB	7.68TB	15.36TB
12V Supply Voltage Tolerance	12V±10%			
12V Rise Time (Max/Min)	1s/1ms			
12V Fall Time (Max/Min)	1s/1ms			
12V Allowable Noise Level	DC to 100Khz : 450mVp-p Max 100Khz to 220Mhz : 350mVp-p Max			
Minimum Off Time	10ms			
3.3Vaux Supply Voltage Tolerance	3.3V±15%			
3.3Vaux Rise time (Max/Min)	50 ms/1 ms			
3.3Vaux Fall Time (Max/Min)	5 ms/1 ms			
3.3Vaux Noise level	300 mV pp 10Hz – 100 KHz 50 mV pp 100KHz – 20 MHz			

NOTE:
1) The components inside SSD were designed to endure the range of voltage fluctuations, which might be induced by the host system, in Table 8.

2.6.2 Power Consumption (12V)

[Table 9] Power Consumption (12V Supply Voltage)

Power Mode			1.92TB	3.84TB	7.68TB	15.36TB
PCIe Gen.5	Active[1]	Read	19.5W	21.0W	21.5W	22.5W
		Write	15.5W	21.5W	21.5W	24.0W
	Idle		8W	8W	8W	8W

NOTE:
1) Typical Power Consumption (Maximum average power with a measurement period of 500ms.).

2.7 Reliability

The reliability specification of the Samsung SSD PM1743 follows JEDEC standard, which are included in JESD218A and JESD219A documents.

2.7.1 Mean Time Between Failures

By definition, Uncorrectable Bit Error Rate (UBER) is a metric for the rate of occurrence of data errors, equal to the number of data errors per bits read as specified in the JESD218 document of JEDEC standard.

[Table 10] MTBF Specifications

Parameter	1.92TB	3.84TB	7.68TB	15.36TB
MTBF	2,000,000 Hours			

2.7.2 Uncorrectable Bit Error Rate

By definition, Uncorrectable Bit Error Rate (UBER) is a metric for the rate of occurrence of data errors, equal to the number of data errors per bits read as specified in the JESD218 document of JEDEC standard.

[Table 11] UBER Specifications

Parameter	1.92TB	3.84TB	7.68TB	15.36TB
UBER	1 sector per 10^{17} bits read			

NOTE:
1) For the enterprise application, JEDEC recommends that UBER shall be below 10^{-16}

2.7.3 Data Retention

By definition, data retention is the expected time period for retaining data in the SSD at the maximum rated endurance in power-off state as specified in the JESD218 document of JEDEC standard.

[Table 12] Data Retention

Parameter	1.92TB	3.84TB	7.68TB	15.36TB
Data Retention[1]	3 months			

NOTE:
1) Data retention was measured by assuming that SSD reaches the maximum rated endurance at 40°C in power-off state.

2.7.4 Endurance

By definition, the endurance of SSD in enterprise application is defined as the maximum number of drive writes per day that can meet the requirements specified in the JESD218 document of JEDEC standard.

[Table 13] Drive Write Per Day (DWPD)

Parameter	1.92TB	3.84TB	7.68TB	15.36TB
DWPD	1 drive writes per day over 5 years			

[Table 14] Petabyte Written (PBW)

Parameter	Unit	1.92TB	3.84TB	7.68TB	15.36TB
PBW	PB	3.504 PB	7.008 PB	14.016 PB	28.032 PB

NOTE:
1) Relational formula between DWPD and PBW is like below:
PBW = DWPD x 365 x 5 x User capacity
2) PBW was calculated at 4KB random write.
3) 1PB = 10^{15} Bytes

2.8 Protection Function

2.8.1 Power Loss Protection

By using internal back-up power technology, the Samsung SSD PM1743 supports power loss protection (PLP) feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

2.8.2 Inrush Current Protection

When the Samsung SSD PM1743 plugs in the backplane of host system, the significant amount of current is induced through 12V power rail.
The Samsung SSD PM1743 has protection circuitry including a set of resisters and capacitors to alleviate the impact by inrush current through 12V power.

[Table 15] Inrush Current

Inrush Current	1.92TB	3.84TB	7.68TB	15.36TB
12 V	1.8A[1)]			

NOTE:
1) The measurement value of inrush current is also compatible with the standard specification of “Enterprise SSD Form Factor Version 1.0a” released by SSD Form Factor Working Group.

2.9 Environmental Specification

2.9.1 Temperature

[Table 16] Temperature, Case (Tc[1])

		1.92TB	3.84TB	7.68TB	15.36TB
Temperature[1)]	Operating	0 to 70°C			
	Non-Operating[2)]	-40 to 85°C			

NOTE:
1) Case temperature (Tcase(Tc)) based on the hottest point on the external case surface.
Highly recommending sufficient airflow to operate properly on heavier workload within the operating temperature.
Performance throttling will be engaged at higher temperature (Tcomp 80?) over the operating temperature.
2) Storing (or shipping) without power connection.

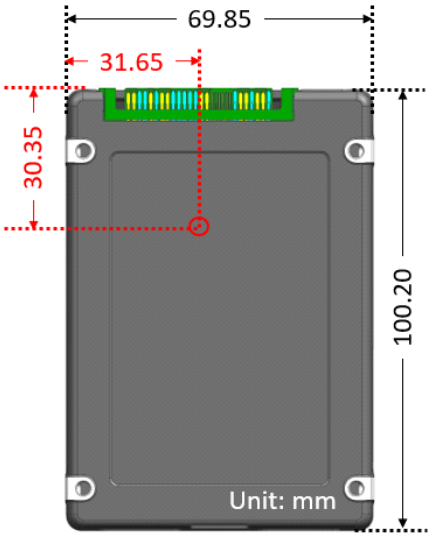


Figure 1. Tc point(1.92TB, 3.84TB, 7.68TB)

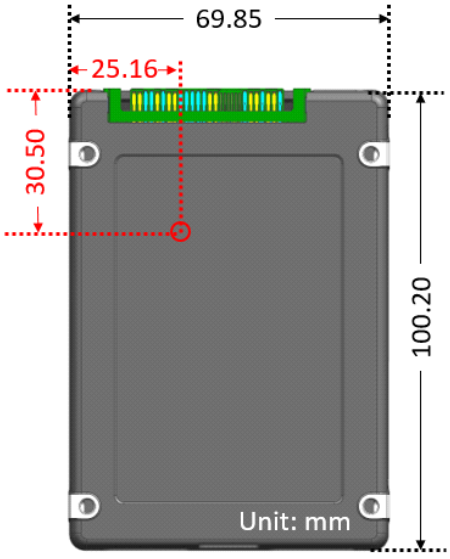


Figure 2. Tc point(15.36TB)

2.9.2 Dynamic Thermal Throttling

The dynamic thermal throttling (DTT) is implemented to prevent overheating. Table 17 shows the engaging and recovery temperature thresholds.

2.9.2.1 DTT Table

[Table 17] DTT Table

DTT Threshold[1), 2)]		1.92TB, 3.84TB, 7.68TB, 15.36TB	Throttled Performance[3)]
DTT1	Warning Composite Temperature (WCTEMP)	80°C	<75%
DTT2	-	84°C	<50%
DTT3	-	86°C	<25%
Critical (DTT4)	Critical Composite Temperature (CCTEMP)	87°C	0%
Shut-down[4)]	-	92°C	n/a

NOTE:
1) All temperatures are based on the composite temperatures (Tcomp).
2) Recovering to the previous step as the temperature falls by 1? for its threshold except thermal shut-down.
3) Throttling levels could be varied with workloads and capacities.
4) Hanged/Halted. Recovering after power cycle only.

2.9.2.2 Composite temperature (Tcomp; $T_{composite}$)

Tcomp is defined by the correlation equation as follows:

Tcomp = TS

where, TS means the reading temperature from the standard thermal sensor on the drive.

2.9.3 Humidity

[Table 18] Humidity

		1.92TB	3.84TB	7.68TB	15.36TB
Humidity[1]	Non-operating	5% to 95%			

NOTE:
1) Humidity is measured in non-condensing state.

2.9.4 Shock and Vibration

[Table 19] Shock and Vibration

Parameter		1.92TB	3.84TB	7.68TB	15.36TB
Shock[1]	Non-operating	1,500G			
Vabration[2]	Non-operating	20 Geak (20~2,000Hz, Sweep sine)			

NOTE:
1) Shock specifications assume that SSD shall be mounted with screws when input vibration is applied.
Vibration may be applied in 3 axes (x, y and z) with a half sine waveform of 0.5ms duration in non-operating condition.
2) Vibration specifications assume that SSD shall be mounted with screws when input vibration is applied.
The input vibration may be applied in 3 axes (x, y and z).

3.0 MECHANICAL SPECIFICATIONS

3.1 Physical Information

The physical case of the Samsung SSD PM1743 in 2.5-inch form factor follows the standardized dimensions defined by SSD Form Factor Work Group.

[Table 20] Physical Dimensions and Weight

Parameter	Unit	1.92TB	3.84TB	7.68TB	15.36TB
Width	mm	69.85±0.25			
Length	mm	100.20±0.25			
Thickness	mm	15.00 + 0.00/-0.50			
Weight	g	Up to 190g			

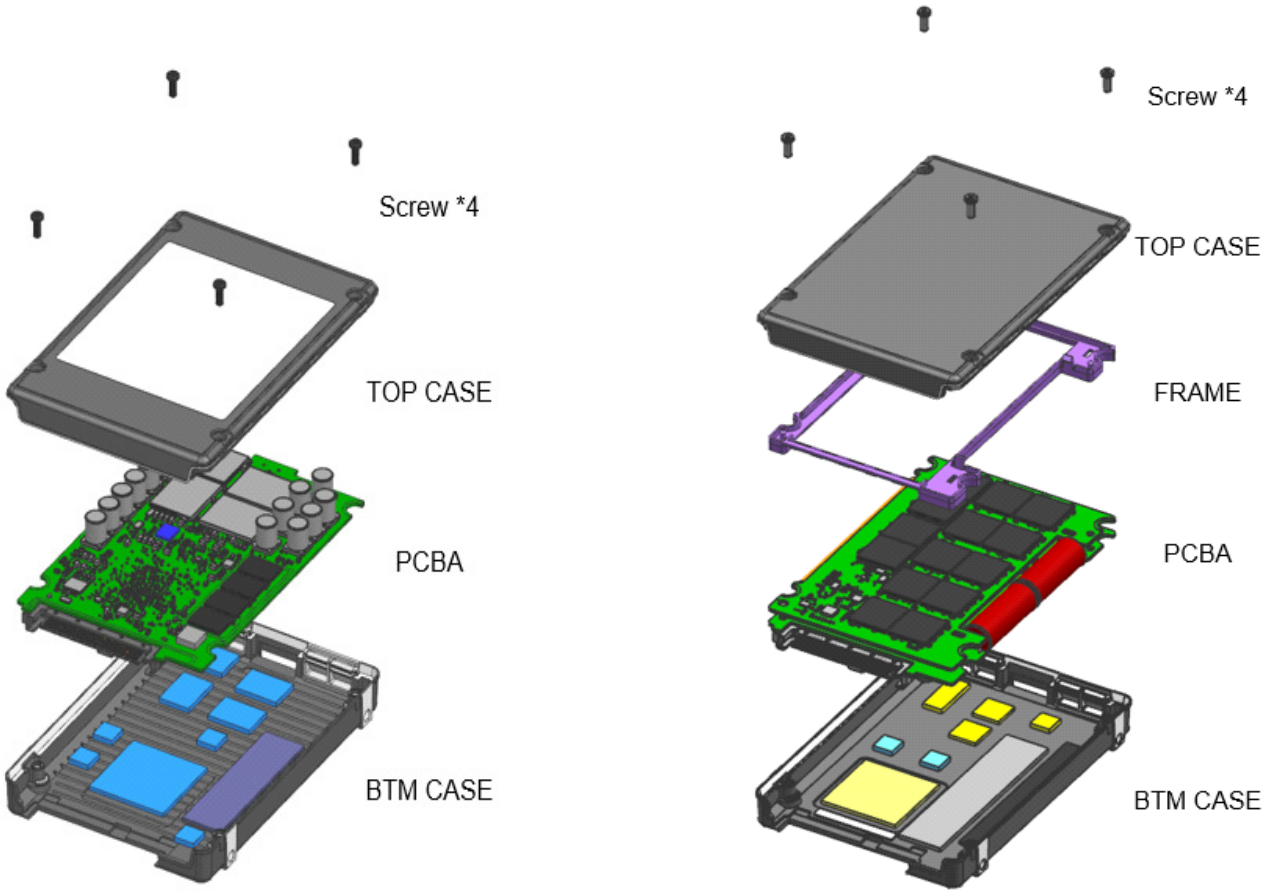
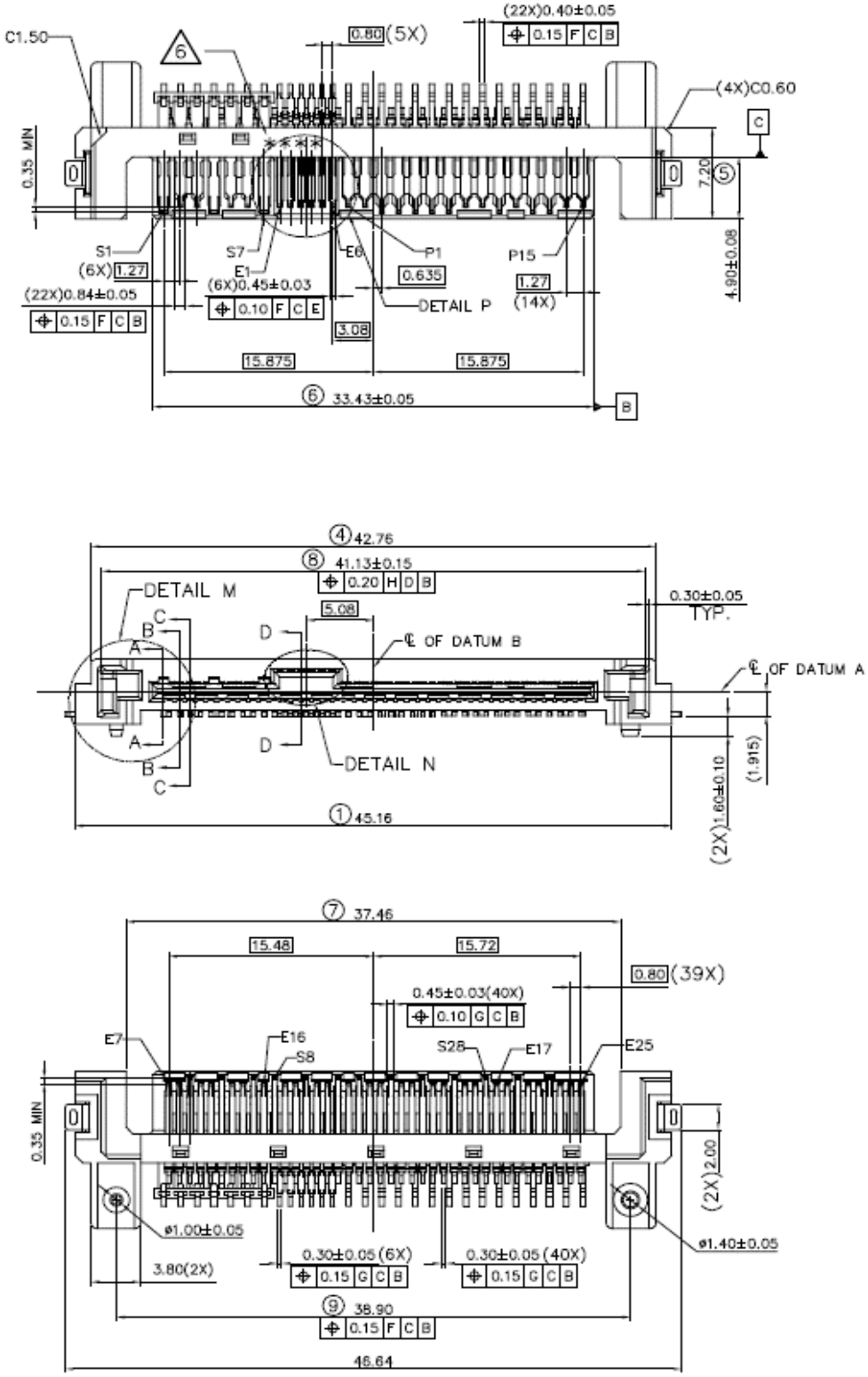


Figure 3. Mechanical Outline

4.0 INTERFACE SPECIFICATION

The PCIe connector of PM1743 is compliant with SFF-8639 standard specification.

4.1 Connector Dimensions



4.2 Connector Pin Assignments and Description

[Table 21] U.2 Pin Assignments and Description

Pin #	Assignment	Description	Pin #	Assignment	Description
S1	GND	Ground	E7	REFCLK+	Reference clock + for first A-Side port
S2	Not Used	Reserved for U.3[4)]	E8	REFCLK-	Reference clock - for first A-Side port
S3	Not Used	Reserved for U.3[4)]	E9	GND	Ground
S4	GND	Ground	E10	PERp0	PCIe Receive+ (lane 0)
S5	Not Used	Reserved for U.3[4)]	E11	PERn0	PCIe Receive- (lane 0)
S6	Not Used	Reserved for U.3[4)]	E12	GND	Ground
S7	GND	Ground	E13	PETn0	PCIe Transmit- (lane 0)
E1	REFCLK1+	Reference clock + for second B-Side port	E14	PETp0	PCIe Transmit+ (lane 0)
E2	REFCLK1-	Reference clock - for second B-Side port	E15	GND	Ground
E3	3.3V AUX	3.3V Auxiliary Power	E16	HPT1	Host Port Type 1
E4	PERSTB#	PCIe Reset for second B-Side port	S8	Not Used	Ground
E5	PERST#	PCIe Reset for first A-Side port	S9	Not Used	Reserved for U.3[4)]
E6	IfDet2#	Ground	S10	Not Used	Reserved for U.3[4)]
P1	WAKE#	NC (Not connected)	S11	Not Used	Ground
P2	Not Used	NC (Not connected)	S12	Not Used	Reserved for U.3[4)]
P3	PWRDIS	Power Disable	S13	Not Used	Reserved for U.3[4)]
P4	IfDet#	Ground	S14	Not Used	Ground
P5	GND	Ground	S15	HPT0	Host Port Type 0 [5]
P6	GND	Ground	S16	GND	Ground
P7	Not Used	P7, P8 and P9 are tied together	S17	PERp1	PCIe Receive+ (lane 1)
P8	Not Used	P7, P8 and P9 are tied together	S18	PERn1	PCIe Receive- (lane 1)
P9	Not Used	P7, P8 and P9 are tied together	S19	GND	Ground
P10	PRSNT#	NC (Not connected)	S20	PETn1	PCIe Transmit- (lane 1)
P11	ACTIVITY#	Device Activity	S21	PETp1	PCIe Transmit+ (lane 1)
P12	GND	Ground	S22	GND	Ground
P13	12V Precharge	12V Precharge Power	S23	PERp2	PCIe Receive+ (lane 2)
P14	12V	12V Primary Power	S24	PERn2	PCIe Receive- (lane 2)
P15	12V	12V Primary Power	S25	GND	Ground
			S26	PETn2	PCIe Transmit- (lane 2)
			S27	PETp2	PCIe Transmit+ (lane 2)
			S28	GND	Ground
			E17	PERp3	PCIe Receive+ (lane 3)
			E18	PERn3	PCIe Receive- (lane 3)
			E19	GND	Ground
			E20	PETn3	PCIe Transmit- (lane 3)
			E21	PETp3	PCIe Transmit+ (lane 3)
			E22	GND	Ground
			E23	SMBCLK	SMBus Clock
			E24	SMBDAT	SMBus Data
			E25	DualPortEn#	Dual Port PCIe enable

NOTE:
1) Names on the pin assignments and description are written from the PCIe device perspective.
2) The PETpx and PETnx pins shall be connected to the PCI Express Receiver differential pair on the host system/platform board.
3) The PERpx and PERnx pins shall be connected to the PCI Express Transmitter differential pair on host system/platform board.
4) Assigned for PCIe transmit/receive and auxiliary signals of U.3 interface support.
5) Determine which type of slot the device mated to. If S15 pin connected to GND through host, the device will operate as U.3 interface.
If slot has no connection(floated) to this pin, the device will operates as U.2(Enterprise SSD Form Factor 1.0a) interface.

5.0 PCI AND NVM EXPRESS REGISTERS

5.1 PCI Express® Configuration Registers

5.1.1 PCI Register Summary

[Table 22] PCI Register Summary

Start Address	Tag	Name	Type
00h	TYPE0_HDR	PCI Header	PCI Configuration Header Space
40h	PM_CAP	PCI Power Management Capability	PCI Capability
50h	MSI_CAP	Message Signaled Interrupt Capability	PCI Capability
70h	PCIE_CAP	PCI Express® Capability	PCI Capability
B0h	MSIX_CAP	MSI-X Capability	PCI Capability
100h	AER_CAP	Advanced Error Reporting (AER) Capability	PCIe Extended Capability
148h	DEV_CAP	Device Serial Number Capability	PCIe Extended Capability
168h	ARI_CAP	Alternative Routing-ID (ARI) Capability	PCIe Extended Capability
178h	SPCIE_CAP	Secondary PCI Express® Capability	PCIe Extended Capability
198h	PL16G_CAP	Physical Layer 16.0 GT/s Capability	PCIe Extended Capability
1BCh	MARGIN_CAP	Lane Margining Capability	PCIe Extended Capability
1D4h	PL32G_CAP	Physical Layer 32.0 GT/s Capability	PCIe Extended Capability
3C0h	DLINK_CAP	Data Link Feature Capability	PCIe Extended Capability

5.1.2 PCI Configuration Header Space Registers Detail

5.1.2.1 PCI Configuration Header Space Registers

[Table 23] PCI Header Space Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Status Register
08h	08h	REVID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (Lower 32-bit)
14h	17h	MUBAR (BAR1)	Memory Register Base Address (Upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Reserved
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EXPROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	R	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

[Table 24] Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A826h	Device ID
0:15	RO	144Dh	Vendor ID

[Table 25] Command Register

Bits	Type	Default Value	Description
15:11	RO	0	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back Enable (N/A)
8	RW	0	SERR# Enable
7	RO	0	IDSEL Stepping / Wait Cycle Control (N/A)
6	RW	0	Parity Error Response Enable
5	RO	0	VGA Palette Snooping Enable (N/A)
4	RO	0	Memory Write and Invalidate Enable (N/A)
3	RO	0	Special Cycle Enable (N/A)
2	RW	0	Bus Master Enable
1	RW	0	Memory Space Enable
0	RW	0	I/O Space Enable

[Table 26] Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Detected Parity Error
14	RW1C	0	Signaled System Error
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort (N/A)
10:9	RO	0	DEVSEL Timing (N/A)
8	RW1C	0	Master Data Parity Error Detected (N/A)
7	RO	0	Fast Back-to-Back Transaction Capable (N/A)
6	RO	0	Reserved
5	RO	0	66MHz Capable (N/A)
4	RO	1h	Capabilities List
3	RO	0	Interrupt Status
2:1	RO	0	Reserved
0	RO	0	Reserved

[Table 27] Revision ID Register

Bits	Type	Default Value	Description
7:0	RO	0h	Controller Hardware Revision ID

[Table 28] Class Code Register

Bits	Type	Default Value	Description
23:16	RO	01h	Base Class Code
15:8	RO	08h	Sub Class Code
7:0	RO	02h	Programming Interface

[Table 29] Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0	Cache Line Size (N/A)

[Table 30] Master Latency Timer Register

Bits	Type	Default Value	Description
7:0	RO	0	Master Latency Timer (N/A)

[Table 31] Header Type Register

Bits	Type	Default Value	Description
7	RO	0	Multi-function Device (N/A)
6:0	RO	0	Reserved

[Table 32] Built In Self Test Register

Bits	Type	Default Value	Description
7	RO	0	Built In Self Test (N/A)
6	RO	0	Built In Self Test (N/A)
5:4	RO	0	Built In Self Test (N/A)
3:0	RO	0	Built In Self Test (N/A)

[Table 33] Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:15	RW	0	Base Address
14:4	RO	0	Reserved
3	RO	0	Pre-Fetchable
2:1	RO	2h	Address Type (64-bit)
0	RO	0	Memory Space Indicator (MEMSI)

[Table 34] Memory Register Base Address Upper 32-bits (BAR1)

Bits	Type	Default Value	Description
31:0	RW	0	Base Address

[Table 35] Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 36] BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 37] Vendor Specific BAR4 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 38] Vendor Specific BAR5 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 39] Cardbus CIS Pointer Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 40] Subsystem Identifier Register

Bits	Type	Default Value	Description
31:16	RO	1.92TB: AD0Ah 3.84TB: AD0Bh 7.68TB: AD0Ch 15.36TB: AD0Dh	Subsystem ID
15:0	RO	144Dh	Subsystem Vendor ID

[Table 41] Expansion ROM Register

Bits	Type	Default Value	Description
31:17	RW	0	Expansion ROM Base Address
16:1	RO	0	Reserved
0	RW	0	Expansion ROM Enable/Disable

[Table 42] Capabilities Pointer Register

Bits	Type	Default Value	Description
7:0	RO	40h	Capability Pointer

[Table 43] Interrupt Information Register

Bits	Type	Default Value	Description
1r5:8	RO	01h	Interrupt Pin
7:0	RW	0	Interrupt Line

[Table 44] Minimum Grant Register

Bits	Type	Default Value	Description
7:0	RO	0	Minimum Grant (N/A)

[Table 45] Maximum Latency Register

Bits	Type	Default Value	Description
7:0	RO	0	Maximum Latency (N/A)

5.1.3 PCI Capability Registers

5.1.3.1 PCI Power Management Capability

[Table 46] PCI Power Management Capability Register Summary

Start Address	End Address	Symbol	Description
40h	40h	PCIPM_ID	PCI Power Management Capability ID
41h	41h	NEXTCAP	Next Capability Pointer
42h	43h	PCIPM_CAP	PC Power Management Capabilities
44h	45h	PCIPM_CS	PCI Power Management Control and Status
46h	46h	PCIPM_CSR_BSE	PMCSR_BSE Bridge Extensions
47h	47h	PCIPM_DATA	Data

[Table 47] PCI Power Management Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	50h	Next Capability
7:0	RO	1h	Capability ID

[Table 48] PCI Power Management Capability Register

Bits	Type	Default Value	Description
15:11	RO	0	PME Support (N/A)
10	RO	0	D2 Support (N/A)
9	RO	0	D1 Support (N/A)
8:6	RO	0	AUX current (N/A)
5	RO	0	Device Specific Initialization (N/A)
4	RO	1h	Immediate_Readiness_on_Return_to_D0
3	RO	0	PME Clock (N/A)
2:0	RO	3h	Version (Support for PCIe Power Management Interface Spec revision 1.2)

[Table 49] PCI Power Management Control and Status Register

Bits	Type	Default Value	Description
31:24	RsvdP	0	Data register (N/A)
23	RO	0	Bus Power/Clock Enable (N/A)
22	RO	0	B2, B3 support (N/A)
21:16	RsvdP	0	Reserved
15	RO	0	PME Status (N/A)
14:13	RO	0	Data scale (N/A)
12:9	RO	0	Data scale (N/A)
8	RWS	0	PME Enable (N/A)
7:4	RsvdP	0	Reserved
3	RO	1	No Soft Reset
2	RsvdP	0	Reserved
1:0	RW	0	Power State

5.1.3.2 Message Signaled Interrupt (MSI) Capability

[Table 50] Message Signaled Interrupt Capability Summary

Start Address	End Address	Symbol	Description
50h	51h	MSI_ID	Message Signaled Interrupt Capability ID
52h	53h	MSI_MC	Message Signaled Interrupt Message Control
54h	57h	MSI_MA	Message Signaled Interrupt Message Address
58h	5Bh	MSI_MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MSI_MDATA	Message Signaled Interrupt Message Data
60h	63h	MSI_MMASK	Message Signaled Interrupt Mask Bits
64h	67h	MSI_MPEND	Message Signaled Interrupt Pending Bits

[Table 51] Message Signaled Interrupt Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	70h	Next Capability Pointer
7:0	RO	05h	Capability ID

[Table 52] Message Signaled Interrupt Control Register

Bits	Type	Default Value	Description
15:9	RsvdP	0	Reserved
8	RO	0	Per Vector Masking Capable (N/A)
7	RO	1h	64-bit Address Capable
6:4	RW	0	Multiple Message Enable
3:1	RO	5h	Multiple Message Capable
0	RW	0	MSI Enable

[Table 53] Message Signaled Interrupt Address Register

Bits	Type	Default Value	Description
31:2	RW	0	Address
1:0	RsvdP	0	Reserved

[Table 54] Message Signaled Interrupt Message Upper Address Register

Bits	Type	Default Value	Description
31:0	RW	0	Upper Address

[Table 55] Message Signaled Interrupt Message Data Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15:0	RW	0	Data

[Table 56] Message Signaled Interrupt Message Mask Bits Register

Bits	Type	Default Value	Description
31:0	RW	0	Mask Bits (N/A)

[Table 57] Message Signaled Interrupt Message Pending Bits Register

Bits	Type	Default Value	Description
31:0	RO	0	Pending Bits

5.1.3.3 PCI Express® Capability

[Table 58] PCI Capability Register Summary

Start Address	End Address	Symbol	Description
70h	71h	PCIE_ID	PCI Express® Capability ID
72h	73h	PCIE_CAP	PCI Express® Capabilities
74h	77h	PCIE_DCAP	PCI Express® Device Capabilities
78h	79h	PCIE_DC	PCI Express® Device Control
7Ah	7Bh	PCIE_DS	PCI Express® Device Status
7Ch	7Fh	PCIE_LCAP	PCI Express® Link Capabilities
80h	81h	PCIE_LC	PCI Express® Link Control
82h	83h	PCIE_LS	PCI Express® Link Status
94h	97h	PCIE_DCAP2	PCI Express® Device Capabilities 2
98h	99h	PCIE_DC2	PCI Express® Device Control 2
9Ah	9Bh	PCIE_DS2	PCI Express® Device Status 2
9Ch	9Fh	PCIE_LCAP2	PCI Express® Link Capabilities 2
A0h	A1h	PCIE_LC2	PCI Express® Link Control 2
A2h	A3h	PCIE_LS2	PCI Express® Link Status 2

[Table 59] PCI Express® Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	B0h	Next Capability Pointer
7:0	RO	10h	Capability ID

[Table 60] PCI Express® Capabilities Register

Bits	Type	Default Value	Description
15:14	RsvdP	0	Reserved
13:9	RO	0	Interrupt Message Number
8	HWInit	0	Slot Implementation (N/A)
7:4	RO	0	Device/Port Type
3:0	RO	2h	Capability Version

[Table 61] PCI Express® Device Capabilities Register

Bits	Type	Default Value	Description
31:29	RsvdP	0	Reserved
28	RO	1h	Function Level Reset Capability
27:26	RO	0	Captured Slot Power Limit Scale
25:18	RO	0	Captured Slot Power Limit Value
17:16	RsvdP	0	Reserved
15	RO	1h	Role-based Error Reporting
14:12	RO	0	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	1h	Extended Tag Field Supported
4:3	RO	0	Phantom Functions Supported
2:0	RO	2h	Max Payload Size Supported

[Table 62] PCI Express® Device Control Register

Bits	Type	Default Value	Description
15	RW	0	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	1h	Enable No Snoop
10	RWS	0	Aux Power PM Enable (N/A)
9	RW	0	Phantom Functions Enable (N/A)
8	RW	1h	Extended Tag Enable
7:5	RW	0	Max Payload Size
4	RW	1h	Enable Relaxed Ordering
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

[Table 63] PCI Express® Device Status Register

Bits	Type	Default Value	Description
15:6	RsvdZ	0	Reserved
5	RO	0	Transactions Pending
4	RO	0	Aux Power Detected
3	RW1C	0	Unsupported Request Detected
2	RW1C	0	Fatal Error Detected
1	RW1C	0	Non-Fatal Error Detected
0	RW1C	0	Correctable Error Detected

[Table 64] PCI Express® Link Capabilities Register

Bits	Type	Default Value	Description
31:24	HWInit	0h	Port Number
23	RsvdP	0	Reserved
22	HWInit	1h	ASPM Optionality Compliance
21	RO	0	Link Bandwidth Notification Capability (N/A)
20	RO	0	Data Link Layer Link Active Reporting Capable (N/A)
19	RO	0	Surprise Down Error Reporting Capable (N/A)
18	RO	0	Clock Power Management
17:15	RO	6h	L1 Exit Latency
14:12	RO	7h	L0s Exit Latency
11:10	RO	0	Active State Power Management Support
9:4	RO	Single Port: 4h (x4 link) Dual Port: 2h (x2 link)	Maximum Link Width
3:0	RO	5h	Max Link Speeds

[Table 65] PCI Express® Link Control Register

Bits	Type	Default Value	Description
15:14	RW/RsvdP	0	Reserved
13:12	RsvdP	0	Reserved
11	RsvdP	0	Link Autonomous Bandwidth interrupt enable (N/A)
10	RsvdP	0	Link Bandwidth management interrupt enable (N/A)
9	RW	0	Hardware Autonomous Width Disable
8	RW	0	Enable Clock Power Management
7	RW	0	Extended Sync
6	RW	0	Common Clock Configuration
5	RsvdP	0	Retrain Link (N/A)
4	RsvdP	0	Link Disable (N/A)
3	RW	0	Read Completion Boundary (N/A)
2	RsvdP	0	Reserved
1:0	RW	0	Active State Power Management Control

[Table 66] PCI Express® Link Status Register

Bits	Type	Default Value	Description
15	RsvdP	0	Link Autonomous Bandwidth Status (N/A)
14	RsvdP	0	Link Bandwidth Management Status (N/A)
13	RO	0	Data Link Layer Link Active
12	HWInit	1h	Slot Clock Configuration
11	RO	0	Link Training (N/A)
10	RO	0	Reserved
9:4	RO	1h	Negotiated Link Width
3:0	RO	1h	Current Link Speed

[Table 67] PCI Express® Device Capabilities 2 Register

Bits	Type	Default Value	Description
31	HWInit	1h	FRS Supported
30:24	RsvdP	0	Reserved
23:22	HWInit	0	Max End-End TLP Prefixes (N/A)
21	HWInit	0	End-End TLP Prefix Supported (N/A)
20	RO	0	Extended Format Field Supported (N/A)
19:18	HWInit	0	OBFF Supported (N/A)
17	HWInit	0	10-Bit Tag Requester Supported
16	HWInit	1h	10-Bit Tag Completer Supported
15:14	HWInit	0	LN System CLS (N/A)
13:12	RO	0	TPH Completer Supported (N/A)
11	RO	1h	Latency Tolerance Reporting Supported
10	HWInit	0	No RO-enabled PR-PR Passing (N/A)
9	RO	0	128-bit CAS Completer Supported (N/A)
8	RO	0	64-bit Atomic Op Completer Supported (N/A)
7	RO	0	32-bit Atomic Op Completer Supported (N/A)
6	RO	0	Atomic Op Routing Supported (N/A)
5	RO	0	ARI Forwarding Supported (N/A)
4	RO	1h	Completion Timeout Disable Supported
3:0	HWInit	Fh	Completion Timeout Ranges Supported

[Table 68] PCI Express® Device Control 2 Register

Bits	Type	Default Value	Description
15	RsvdP	0	End-to-end TLP Prefix Blocking (N/A)
14:13	RW/RsvdP	0	OBFF Enable (N/A)
12:11	RsvdP	0	Reserved
10	RW/RsvdP	0	Latency Tolerance Reporting Mechanism Enable
9	RW	0	IDO Completion enable (N/A)
8	RW	0	IDO Request Enable (N/A)
7	RW	0	AtomicOp Egress Blocking (N/A)
6	RW	0	AtomicOp Requester Enable (N/A)
5	RW	0	ARI forwarding supported (N/A)
4	RW	0	Completion Timeout Disable
3:0	RW	0	Completion Timeout Value

[Table 69] PCI Express® Device Status 2 Register

Bits	Type	Default Value	Description
15:0	RsvdZ	0	Reserved

[Table 70] PCI Express® Link Capabilities 2 Register

Bits	Spec Tpye	Default Value	Description
31	RO	1h	DRS support
30:25	RsvdP	0	Reserved
24	RsvdP	1h	Two Retimers Presence Detect Supported
23	HwInit	1h	Retimer Presence Detect Supported
22:16	HwInit	0	Lower SKP OS Reception Supported Speed Vector (N/A)
15:9	HwInit	0	Lower SKP OS Generation Supported Speed Vector (N/A)
8	RO	0	Cross-Link Supported (N/A)
7:1	RO	1Fh	Supported Speeds Vector
0	RsvdP	0	Reserved

[Table 71] PCI Express® Link Control 2 Register

Bits	Type	Default Value	Description
15:12	RWS/RsvdP	0	Compliance De-emphasis
11	RWS/RsvdP	0	Compliance SOS
10	RWS/RsvdP	0	Enter Modified Compliance
9:7	RWS/RsvdP	0	Transmit Margin
6	HWInit	0	Select De-Emphasis (N/A)
5	RWS/RsvdP	0	Hardware Autonomous Speed Disable
4	RWS/RsvdP	0	Enter Compliance
3:0	RWS/RsvdP	5h	Target Link Speed

[Table 72] PCI Express® Link Status 2 Register

Bits	Type	Default Value	Description
15:10	RsvdP	0	Reserved
9:8	RO	1h	Crosslink Resolution
7:6	RsvdP	0	Reserved
5	RW1CS	0	Link Equalization Request 8.0GT/s
4	ROS	0	Equalization 8.0GT/s Phase 3 Successful
3	ROS	0	Equalization 8.0GT/s Phase 2 Successful
2	ROS	0	Equalization 8.0GT/s Phase 1 Successful
1	ROS	0	Equalization 8.0GT/s Complete
0	RO	1h	Current De-Emphasis

5.1.3.4 MSI-X Capability

[Table 73] MSI-X Capability Summary

Start Address	End Address	Symbol	Description
B0h	B1h	MSIX_ID	MSI-X Capability ID
B2h	B3h	MSIX_CAP	MSI-X Message Control
B4h	B7h	MSIX_TBL	MSI-X Table Offset and Table BIR
B8h	BBh	MSIX_PBA	MSI-X PBA Offset and PBA BIR

[Table 74] MSI-X Identifier Register

Bits	Type	Default Value	Description
15:8	RO	00h	Next Capability Pointer
7:0	RO	11h	Capability ID

[Table 75] MSI-X Control Register

Bits	Type	Default Value	Description
15	RW	0	MSI-X Enable
14	RW	0	Function Mask
13:11	RsvdP	0	Reserved
10:0	RO	7Fh	Table Size

[Table 76] MSI-X Table Offset Register

Bits	Type	Default Value	Description
31:3	RO	800h	Table Offset
2:0	RO	0	Table BIR

[Table 77] MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value	Description
31:3	RO	600h	Pending Bit Array Offset
2:0	RO	0	Pending Bit Array BIR

5.1.4 PCI Extended Capability Details

5.1.4.1 Advanced Error Reporting Registers

[Table 78] Advanced Error Reporting Capability Summary

Start Address	End Address	Symbol	Description
100h	103h	AER_ID	AER Capability ID
104h	107h	AER_UCES	AER Uncorrectable Error Status
108h	10Bh	AER_UCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AER_UCESEV	AER Uncorrectable Error Severity
110h	113h	AER_CES	AER Correctable Error Status
114h	117h	AER_CEM	AER Correctable Error Mask
118h	11Bh	AER_CC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AER_HL	AER Header Log

[Table 79] AER Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	148h	Next Capability Pointer
19:16	RO	2h	Capability Version
15:0	RO	1h	Capability ID

[Table 80] AER Uncorrectable Error Status Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0	Reserved
26	RW1CS	0	Poisoned TLP Egress Blocked Status (N/A)
25	RW1CS	0	TLP Prefix Blocked Error Status (N/A)
24	RW1CS	0	Atomic Op Egress Blocked Status (N/A)
23	RW1CS	0	MC Blocked TLP Status (N/A)
22	RW1CS	0	Uncorrectable Internal Error Status
21	RW1CS	0	ACS Violation Status (N/A)
20	RW1CS	0	Unsupported Request Error Status
19	RW1CS	0	ECRC Error Status
18	RW1CS	0	Malformed TLP Status
17	RW1CS	0	Receiver Overflow Status
16	RW1CS	0	Unexpected Completion Status
15	RW1CS	0	Completer Abort Status
14	RW1CS	0	Completion Timeout Status
13	RW1CS	0	Flow Control Protocol Error Status
12	RW1CS	0	Poisoned TLP Status
11:6	RsvdZ	0	Reserved
5	RW1CS	0	Surprise Down Error Status (N/A)
4	RW1CS	0	Data Link Protocol Error Status
3:1	RsvdZ	0	Reserved
0	Undefined	0	Undefined

[Table 81] AER Uncorrectable Error Mask Register

Bits	Type	Default Value	Description
31:27	RsvdP	0	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Mask (N/A)
25	RWS	0	TLP Prefix Blocked Error Mask (N/A)
24	RWS	0	Atomic Op Egress Blocked Mask (N/A)
23	RWS	0	MC Blocked TLP Mask (N/A)
22	RWS	1h	Uncorrectable Internal Error Mask
21	RWS	0	ACS Violation Mask (N/A)
20	RWS	0	Unsupported Request Error Mask
19	RWS	0	ECRC Error Mask
18	RWS	0	Malformed TLP Mask
17	RWS	0	Receiver Overflow Mask
16	RWS	0	Unexpected Completion Mask
15	RWS	0	Completer Abort Mask
14	RWS	0	Completion Timeout Mask
13	RWS	0	Flow Control Protocol Error Mask
12	RWS	0	Poisoned TLP Mask
11:6	RsvdP	0	Reserved
5	RWS	0	Surprise Down Error Mask (N/A)
4	RWS	0	Data Link Protocol Error Mask
3:1	RsvdP	0	Reserved
0	Undefined	0	Undefined

[Table 82] AER Uncorrectable Error Severity Register

Bits	Type	Default Value	Description
31:27	RsvdP	0	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Severity (N/A)
25	RWS	0	TLP Prefix Blocked Error Severity (N/A)
24	RWS	0	Atomic Op Egress Blocked Severity (N/A)
23	RWS	0	MC Blocked TLP Severity (N/A)
22	RWS	1h	Uncorrectable Internal Error Severity
21	RWS	0	ACS Violation Severity (N/A)
20	RWS	0	Unsupported Request Error Severity
19	RWS	0	ECRC Error Severity
18	RWS	1h	Malformed TLP Severity
17	RWS	1h	Receiver Overflow Severity
16	RWS	0	Unexpected Completion Severity
15	RWS	0	Completer Abort Severity
14	RWS	0	Completion Timeout Severity
13	RWS	1h	Flow Control Protocol Error Severity
12	RWS	0	Poisoned TLP Severity
11:6	RsvdP	0	Reserved
5	RWS	1h	Surprise Down Error Severity (N/A)
4	RWS	1h	Data Link Protocol Error Severity
3:1	RsvdP	0	Reserved
0	Undefined	0	Undefined

[Table 83] AER Correctable Error Status Register

Bits	Type	Default Value	Description
31:16	RsvdZ	0	Reserved
15	RW1CS	0	Header Log Overflow Status
14	RW1CS	0	Corrected Internal Error Status
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status
11:9	RsvdZ	0	Reserved
8	RW1CS	0	Replay Number Rollover Status
7	RW1CS	0	Bad DLLP Status
6	RW1CS	0	Bad TLP Status
5:1	RsvdZ	0	Reserved
0	RW1CS	0	Received Error Status

[Table 84] AER Correctable Error Mask Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15	RWS	1h	Header Log Overflow Mask
14	RWS	1h	Corrected Internal Error Mask
13	RWS	1h	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask
11:9	RsvdP	0	Reserved
8	RWS	0	Replay Number Rollover Mask
7	RWS	0	Bad DLLP Mask
6	RWS	0	Bad TLP Mask
5:1	RsvdP	0	Reserved
0	RWS	0	Received Error Mask

[Table 85] AER Capabilities and Control Register

Bits	Type	Default Value	Description
31:13	RsvdP	0	Reserved
12	RO	0	Completion Timeout Prefix/Header Log Capable (N/A)
11	ROS	0	TLP Prefix Log Present (N/A)
10	RWS	0	Multiple Header Recording Enable
9	RO	1h	Multiple Header Recording Capable
8	RWS	0	ECRC Check Enable
7	RO	1h	ECRC Check Capable
6	RWS	0	ECRC Generation Enable
5	RO	1h	ECRC Generation Capable
4:0	ROS	0	First Error Pointer

[Table 86] AER Header Log Register

Bits	Type	Default Value	Description
127:120	ROS	0	Header Byte 0
119:112	ROS	0	Header Byte 1
111:104	ROS	0	Header Byte 2
103:96	ROS	0	Header Byte 3
95:88	ROS	0	Header Byte 4
87:80	ROS	0	Header Byte 5
79:72	ROS	0	Header Byte 6
71:64	ROS	0	Header Byte 7
63:56	ROS	0	Header Byte 8
55:48	ROS	0	Header Byte 9
47:40	ROS	0	Header Byte 10
39:32	ROS	0	Header Byte 11
31:24	ROS	0	Header Byte 12
23:16	ROS	0	Header Byte 13
15:8	ROS	0	Header Byte 14
7:0	ROS	0	Header Byte 15

5.1.5 Device serial number capability registers

[Table 87] Device serial number capability Summary

Start Address	End Address	Symbol	Description
148h	14Bh		Device Serial Number Extended Capability Header
14Ch	14Fh		Serial Number Register (Lower DW)
150h	153h		Serial Number Register (Upper DW)

[Table 88] Device Serial Number Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	168h	Next Capability Pointer
19:16	HwInit	1h	Capability Version
15:0	HwInit	3h	Serial number capability ID (Secondary PCI Express Extended capability)

[Table 89] Device Serial Number Register (Upper and Lower DW)

Bits	Type	Default Value	Description
63:0	RO	0	Device serial number register

5.1.5.1 Alternative Routing-ID(ARI) Capability

[Table 90] Alternative Routing-ID(ARI) Capability Summary

Start Address	End Address	Symbol	Description
168h	16Bh		Alternative Routing-ID(ARI) Capability Header
16Ch	16Dh		ARI Capability Register
16Eh	16Fh		ARI Control Register

[Table 91] Alternative Routing-ID(ARI) Capability Header

Bits	Type	Default Value	Description
31:20	RO	178h	Next Capability Pointer
19:16	RO	1h	Capability Version
15:0	RO	Eh	PCI Express Extended Capability ID

[Table 92] ARI Capability Register

Bits	Type	Default Value	Description
15:8	RO	1h	Next Function Number
7:2	RO	0	RsvdP
1	RO	1h	ACS Function Groups Capability
0	RO	0	MFVC Function Groups Capability

[Table 93] ARI Control Register

Bits	Type	Default Value	Description
15:7	RsvdP	0	RsvdP
6:4	RW	0	Function Group
3:2	RsvdP	0	RsvdP
1	RW	0	ACS Function Groups Enable
0	RW	0	MFVC Function Groups Enable

5.1.5.2 Secondary PCI Express® Capability

[Table 94] Secondary PCI Express® Capability Summary

Start Address	End Address	Symbol	Description
178h	17Bh	SPE_ID	Secondary PCI Express® Capability
17Ch	17Fh	SPE_LC3	PCI Express® Link Control 3
180h	183h	SPE_LE	PCI Express® Lane Error Status
184h	185h	SPE_L0EC	PCI Express® Lane 0 Equalization Control
186h	187h	SPE_L1EC	PCI Express® Lane 1 Equalization Control
188h	189h	SPE_L2EC	PCI Express® Lane 2 Equalization Control
18Ah	18Bh	SPE_L3EC	PCI Express® Lane 3 Equalization Control

[Table 95] Secondary PCI Express Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	198h	Next Capability Pointer
19:16	RO	1h	Capability Version
15:0	RO	19h	Capability ID (Secondary PCI Express Extended capability)

[Table 96] PCI Express® Link Control 3 Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15:9	RW	0	Enable Lower SKP OS Generation Vector (N/A)
8:2	RsvdP	0	Reserved
1	RW	0	Link Equalization Request Interrupt Enable (N/A)
0	RW	0	Perform Equalization (N/A)

[Table 97] PCI Express® Lane Error Status Register

Bits	Type	Default Value	Description
31:4	RsvdP	0	Reserved
3:0	RW1CS	0	Lane Error Status Bits

[Table 98] Lane 0 Equalization Control Register

Bits	Type	Default Value	Description
15	RsvdP	0	Upstream Port 8.0T/s Receiver Preset Hint
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Transmitter Preset
11:8	HwInit/RO	4h	Reserved
7	RdvdZ	0	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
6:4	HwInit/RsvdP	0	
3:0	HwInit/RsvdP	0	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 99] Lane 1 Equalization Control Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	4h	Upstream Port 8.0T/s Transmitter Preset
7	RdvdZ	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 100] Lane 2 Equalization Control Register (This is only available for U.2 Single Port)

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	4h	Upstream Port 8.0T/s Transmitter Preset
7	RdvdZ	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 101] Lane 3 Equalization Control Register (This is only available for U.2 Single Port)

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	4h	Upstream Port 8.0T/s Transmitter Preset
7	RdvdZ	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port 8.0T/s Transmitter Preset (N/A)

5.1.6 Physical Layer 16.0 GT/s Capability

[Table 102] Physical Layer 16.0 GT/s Capability Summary

Start Address	End Address	Symbol	Description
198h	19Bh		Physical Layer 16.0 GT/s Extended Capability Header
19Ch	19Fh		16.0 GT/s Capabilities Register
1A0h	1A3h		16.0 GT/s Control Register
1A4h	1A7h		16.0 GT/s Status Register
1A8h	1ABh		16.0 GT/s Local Data Parity Mismatch Status Register
1ACh	1AFh		16.0 GT/s First Retimer Data Parity Mismatch Status Register
1B0h	1B3h		16.0 GT/s Second Retimer Data Parity Mismatch Status Register
1B4h	1B7h		Reserved
1B8h	1BBh		16.0 GT/s Control Register for Lane 0-3

[Table 103] Physical Layer 16.0 GT/s Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	1BCh	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	26h	Capability ID (Secondary PCI Express Extended capability)

[Table 104] 16.0 GT/s Capabilities Register

Bits	Type	Default Value	Description
31:0	RsvdP	0	Reserved

[Table 105] 16.0 GT/s Control Register

Bits	Type	Default Value	Description
31:0	RsvdP	0	Reserved

[Table 106] 16.0 GT/s Status Register

Bits	Type	Default Value	Description
31:5	RsvdZ	0	Reserved
4	RW1CS	0	Link Equalization Request 16.0 GT/s
3	ROS	0	Equalization 16.0 GT/s Phase 3 Successful
2	ROS	0	Equalization 16.0 GT/s Phase 2 Successful
1	ROS	0	Equalization 16.0 GT/s Phase 1 Successful
0	ROS	0	Equalization 16.0 GT/s Complete

[Table 107] 16.0 GT/s Local Data Parity Mismatch Status Register

Bits	Type	Default Value	Description
31:4	RsvdP	0	Reserved
3:0	RW1CS	0	Local Data Parity Mismatch Status

[Table 108] 16.0 GT/s First Retimer Data Parity Mismatch Status Register

Bits	Type	Default Value	Description
31:4	RsvdP	0	Reserved
3:0	RW1CS	0	First Retimer Data Parity Mismatch Status

[Table 109] 16.0 GT/s Second Retimer Data Parity Mismatch Status Register

Bits	Type	Default Value	Description
31:4	RsvdP	0	Reserved
3:0	RW1CS	0	Second Retimer Data Parity Mismatch Status

[Table 110] Reserved

Bits	Type	Default Value	Description
31:0	RsvdP	0	Reserved

[Table 111] 16.0 GT/s Control Register for Lane 0-3

Bits	Type	Default Value	Description
31:28	HwInit/RO	Fh	Upstream Port 16.0 GT/s Transmitter Preset Lane 3
27:24	HwInit/RsvdP	0h	Downstream Port 16.0 GT/s Transmitter Preset Lane 3 (N/A)
23:20	HwInit/RO	Fh	Upstream Port 16.0 GT/s Transmitter Preset Lane 2
19:16	HwInit/RsvdP	0h	Downstream Port 16.0 GT/s Transmitter Preset Lane 2 (N/A)
15:12	HwInit/RO	Fh	Upstream Port 16.0 GT/s Transmitter Preset Lane 1
11:8	HwInit/RsvdP	0h	Downstream Port 16.0 GT/s Transmitter Preset Lane 1 (N/A)
7:4	HwInit/RO	Fh	Upstream Port 16.0 GT/s Transmitter Preset Lane 0
3:0	HwInit/RsvdP	0h	Downstream Port 16.0 GT/s Transmitter Preset Lane 0 (N/A)

5.1.7 Lane Margining Extended Capability

[Table 112] Lane Margining Extended Capability Summary

Start Address	End Address	Symbol	Description
1BCh	1BFh		Margining Extended Capability Header
1C0h	1C3h		Margining Port Capabilities Register
1C4h	1C5h		Margining Port Status Register
1C6h	1C7h		Margining Lane Control Register (Lane 0)
1C8h	1C9h		Margining Lane Status Register (Lane 0)
1CAh	1CBh		Margining Lane Control Register (Lane 1)
1CCh	1CDh		Margining Lane Status Register (Lane 1)
1CEh	1CFh		Margining Lane Control Register (Lane 2)
1D0h	1D1h		Margining Lane Status Register (Lane 2)
1D2h	1D3h		Margining Lane Control Register (Lane 3)
1D4h	1D5h		Margining Lane Status Register (Lane 3)

[Table 113] Physical Layer 16.0 GT/s Margining Capability Header

Bits	Type	Default Value	Description
31:20	RO	1D4h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	27h	PCI Express Extended Capability ID

[Table 114] Margining Port Capabilities Register

Bits	Type	Default Value	Description
15:1	RsvdP	0	Reserved
0	HWInit	0	Margining uses Driver Software

[Table 115] Margining Port Status Register

Bits	Type	Default Value	Description
15:2	RsvdP	0	Reserved
1	RO	1h	Margining Software Ready
0	RO	1h	Margining Ready

[Table 116] Margining Lane Control Register Lane 0

Bits	Type	Default Value	Description
15:8	RW	9Ch	Margin Payload
7	RsvdP	0	Reserved
6	RW	0	Usage Model
5:3	RW	7h	Margin Type
2:0	RW	0	Receiver Number

[Table 117] Margining Lane Status Register Lane 0

Bits	Type	Default Value	Description
15:8	RW	0	MarginPayload Status
7	RsvdP	0	Reserved
6	RW	0	Usage Model Status
5:3	RW	0	Margin Type Status
2:0	RW	0	Receiver Number Status

[Table 118] Margining Lane Control Register Lane 1

Bits	Type	Default Value	Description
15:8	RW	9Ch	Margin Payload
7	RsvdP	0	Reserved
6	RW	0	Usage Model
5:3	RW	7h	Margin Type
2:0	RW	0	Receiver Number

[Table 119] Margining Lane Status Register Lane 1

Bits	Type	Default Value	Description
15:8	RW	0	MarginPayload Status
7	RsvdP	0	Reserved
6	RW	0	Usage Model Status
5:3	RW	0	Margin Type Status
2:0	RW	0	Receiver Number Status

[Table 120] Margining Lane Control Register Lane 2

Bits	Type	Default Value	Description
15:8	RW	9Ch	Margin Payload
7	RsvdP	0	Reserved
6	RW	0	Usage Model
5:3	RW	7h	Margin Type
2:0	RW	0	Receiver Number

[Table 121] Margining Lane Status Register Lane 2

Bits	Type	Default Value	Description
15:8	RW	0	MarginPayload Status
7	RsvdP	0	Reserved
6	RW	0	Usage Model Status
5:3	RW	0	Margin Type Status
2:0	RW	0	Receiver Number Status

[Table 122] Margining Lane Control Register Lane 3

Bits	Type	Default Value	Description
15:8	RW	9Ch	Margin Payload
7	RsvdP	0	Reserved
6	RW	0	Usage Model
5:3	RW	7h	Margin Type
2:0	RW	0	Receiver Number

[Table 123] Margining Lane Status Register Lane 3

Bits	Type	Default Value	Description
15:8	RW	0	MarginPayload Status
7	RsvdP	0	Reserved
6	RW	0	Usage Model Status
5:3	RW	0	Margin Type Status
2:0	RW	0	Receiver Number Status

5.1.8 Physical Layer 32.0 GT/s Extended Capability

[Table 124] Physical Layer 32.0 GT/s Capability Summary

Start Address	End Address	Symbol	Description
1D4h	1D7h		Physical Layer 32.0 GT/s Extended Capability Header
1D8h	1DBh		32.0 GT/s Capabilities Register
1DCh	1DFh		32.0 GT/s Control Register
1E0h	1E3h		32.0 GT/s Status Register
1E4h	1E7h		Received Modified TS Data 1 Register
1E8h	1EBh		Received Modified TS Data 2 Register
1ECh	1EFh		Transmitted Modified TS Data 1 Register
1F0h	1F3h		Transmitted Modified TS Data 2 Register
1F4h	1F7h		32.0 GT/s Lane Equalization Control Register for Lane 0-3

[Table 125] Physical Layer 32.0 GT/s Extended Capability Header

Bits	Spec Type	Default Value	Description
31:20	RO	3C0h	Next Capability Pointer
19:16	RO	1h	Capability Version
15:0	RO	2Ah	Capability ID (Secondary PCI Express Extended capability)

[Table 126] 32.0 GT/s Capabilities Register

Bits	Spec Type	Default Value	Description
31:11	RO	0	Reserved
10	RO	0	Modified TS Usage Mode 2 Supported - Alternate Protocol
9	RO	0	Modified TS Usage Mode 1 Supported - Training Set Message
8	RW	0	Modified TS Usage Mode 0 Supported - PCI Express
1	RW	h1	No Equalization Needed Supported
0	RW	h1	Equalization bypass to highest rate Supported

[Table 127] 32.0 GT/s Control Register

Bits	Spec Type	Default Value	Description
31:11	RsvdP	0	Reserved
10:8	RO	0	Modified TS Usage Mode Selected
1	RWS	0	No Equalization Needed Disable
0	RWS	0	Equalization bypass to highest rate Disable

[Table 128] 32.0 GT/s Status Register

Bits	Spec Type	Default Value	Description
31:11	RsvdZ	0	Reserved
10	RO	0	No Equalization Needed Received
9	RO	h1	Transmitter Precode Request
8	RO	0	Transmitter Precoding On
7:6	RO	0	Received Enhanced Link Behavior Control
5	RO	0	Modified TS Received
4	RW1C	0	Link Equalization Request 32.0 GT/s
3	ROS	0	Equalization 32.0 GT/s Phase 3 Successful
2	ROS	0	Equalization 32.0 GT/s Phase 2 Successful
1	ROS	0	Equalization 32.0 GT/s Phase 1 Successful
0	ROS	0	Equalization 32.0 GT/s Complete

[Table 129] Received Modified TS Data 1 Register

Bits	Spec Type	Default Value	Description
31:16	RO	0	Received Modified TS Vendor ID
15:3	RO	0	Received Modified TS Information 1
2:0	RO	0	Received Modified TS Usage Mode

[Table 130] Received Modified TS Data 2 Register

Bits	Spec Type	Default Value	Description
31:26	RsvdP	0	Reserved
25:24	RO	0	Alternate Protocol Negotiation Status
23:0	RO	0	Received Modified TS Information 2

[Table 131] Transmitted Modified TS Data 1 Register

Bits	Spec Type	Default Value	Description
31:16	RO	0	Transmitted Modified TS Vendor ID
15:3	RO	0	Transmitted Modified TS Information 1
2:0	RO	0	Transmitted Modified TS Usage Mode

[Table 132] Transmitted Modified TS Data 2 Register

Bits	Spec Tpye	Default Value	Description
31:26	RsvdP	0	Reserved
25:24	RO	0	Alternate Protocol Negotiation Status
23:0	RO	0	Transmitted Modified TS Information 2

[Table 133] 32.0 GT/s Lane Equalization Control Register for Lane 0-3

Bits	Spec Type	Default Value	Description
31:28	HwInit/RO	4h	Upstream Port 32.0 GT/s Transmitter Preset (Lane 3)
27:24	HwInit/RsvdP	0	Downstream Port 32.0 GT/s Transmitter Preset (Lane 3)
23:20	HwInit/RO	4h	Upstream Port 32.0 GT/s Transmitter Preset (Lane 2)
19:16	HwInit/RsvdP	0	Downstream Port 32.0 GT/s Transmitter Preset (Lane 2)
15:12	HwInit/RO	4h	Upstream Port 32.0 GT/s Transmitter Preset (Lane 1)
11:8	HwInit/RsvdP	0	Downstream Port 32.0 GT/s Transmitter Preset (Lane 1)
7:4	HwInit/RO	4h	Upstream Port 32.0 GT/s Transmitter Preset (Lane 0)
3:0	HwInit/RsvdP	0	Downstream Port 32.0 GT/s Transmitter Preset (Lane 0)

5.1.8.1 Data Link Feature Extended Capability

[Table 134] Data Link Feature Extended Summary

Start Address	End Address	Symbol	Description
3C0h	3C3h		Data Link Feature Extended Capability Header
3C4h	3C7h		Data Link Feature Capabilities Register
3C8h	3CFh		Data Link Feature Status Register

[Table 135] Data Link Feature Extended Capability Header

Bits	Spec Type	Default Value	Description
31:20	RO	0	Next Capability Pointer
19:16	RO	1h	Capability Version
15:0	RO	25h	PCI Express Extended Capability ID

[Table 136] Data Link Feature Capabilities Register

Bits	Spec Type	Default Value	Description
31	HwInit	1h	Data Link Feature Exchange Enable
30:23	RsvdP	0	Reserved
22:1	RsvdP	0	Reserved
0	HwInit	1h	Local Scaled Flow Control Supported

5.2 NVM Express Registers

5.2.1 Register Summary

[Table 137] Register Summary

Start Address	End Address	Name	Type
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	NSSR	NVM Subsystem Reset (Optional)
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	EFFh	Reserved	Reserved
F00h	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0TDBL	Completion Queue 0 Head Doorbell (Admin)
...			
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDBL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQyHDBL	Completion Queue y Head Doorbell

5.2.2 Controller Registers

[Table 138] Controller Capabilities

Bits	Type	Name	Default Value	Description
63:56	RO	-	0h	Reserved
55:52	RO	MPSMAX	04h	Memory Page Size Maximum ((2 ^ (12 + MPSMAX)).
51:48	RO	MPSMIN	0	Memory Page Size Minimum (2 ^ (12 + MPSMIN)).
47:45	RO	-	0	Reserved
44:37	RO	CSS	1h	Command Sets Supported 1h: NVM command set
36	RO	NSSRS	1h	NVM Subsystem Reset Supported (NSSRS)
35:32	RO	DSTRD	0	Doorbell Stride 0: Stride of 4 bytes
31:24	RO	TO	50h	Timeout (This field is in 500 millisecond units)
23:19	RO	-	0	Reserved
18:17	RO	AMS	1	Arbitration Mechanism Supported
16	RO	CQR	1	Contiguous Queues Required
15:0	RO	MQES	3FFh	Maximum Queue Entries Supported
Offset 20h, 31:00	RW	NSSRC	1h	NVM Subsystem Reset Control (NSSRC)

[Table 139] Version

Bits	Type	Name	Default Value	Description
31:16	RO	MJR	1h	Major Version Number
15:8	RO	MNR	4h	Minor Version Number
7:00	RO	TER	0h	Tertiary Version Number

NOTE:
The PM1743 supports NVM Express™ version 1.3

[Table 140] Interrupt Mask Set

Bits	Type	Name	Default Value	Description
31:00	RW1S	IVMS	0	Interrupt Vector Mask Set

[Table 141] Interrupt Mask Clear

Bits	Type	Name	Default Value	Description
31:00	RW1C	IVMC	0	Interrupt Vector Mask Clear

[Table 142] Controller Configuration

Bits	Type	Name	Default Value	Description
31:24	RO	-	0	Reserved
23:20	RW	IOCQES	0	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16 byte entry size)
19:16	RW	IOSQES	0	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64 byte entry size)
15:14	RW	SHN	0	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0	Reserved
0	RW	EN	0	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

[Table 143] Controller Status

Bits	Type	Name	Default Value	Description
31:4	RO	-	0	Reserved
3:2	RO	SHST	0	Shutdown Status 0h: Normal operation, no shutdown requested 1h: Shutdown processing occurring 2h: Shutdown processing complete 3h: Reserved
1	RO	CFS	0	Controller Fatal Status
0	RO	RDY	0	1h: Controller ready to process commands 0h: Controller shall not process commands.

[Table 144] Admin Queue Attributes

Bits	Type	Name	Default Value	Description
31:28	RO	-	0	Reserved
27:16	RW	ACQS	0	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's based value)
15:12	RO	-	0	Reserved
11:0	RW	ASQS	0	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's based value)

[Table 145] Admin Submission Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ASQB	0	Admin Submission Queue Base Address
11:0	RO	-	0	Reserved

[Table 146] Admin Completion Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ACQB	0	Admin Completion Queue Base Address
11:0	RO	-	0	Reserved

[Table 147] Submission Queue Tail y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO	-	0	Reserved
15:0	RW	SQT	0	Submission Queue Tail

[Table 148] Completion Queue Head y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO	-	0	Reserved
15:0	RW	CQH	0	Completion Queue Head

6.0 SUPPORTED COMMAND SET

6.1 Admin Command Set

[Table 149] Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page - Error Information (01h) - SMART/Health Information (02h) - Firmware Slot Information (03h, M) - Changed Namespace List (04h) - Commands Supported and Effects (05h) - Device Self-test (06h) - Telemetry Host-Initiated (07h) - Telemetry Controller-Initiated (08h) - Interrupt Vector Configuration (09h) - Write Atomicity (0Ah) - Asynchronous Event Configuration (0Bh) - Persistent Event Log (0Dh) - Reservation Notification (80h) - Sanitize Status (81h)
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature - Arbitration (01h) - Power Management (02h) - LBA Range Type (03h) - Temperature Threshold (04h) - Error Recovery (05h) - Number of Queues (07h) - Interrupt Coalescing (08h) - Interrupt Vector Configuration (09h) - Write Atomicity (0Ah) - Asynchronous Event Configuration (0Bh) - Timestamp (0Eh) - LBA Status Information Report Interval(15h) - Sanitize Config(17h) - Software Progress Marker (80h) - Host Identifier (81h) - NS Write Protection Config (84h)
0Ah	Get Feature - Arbitration (01h) - LBA Range Type (03h) - Temperature Threshold (04h) - Error Recovery (05h) - Number of Queues (07h) - Interrupt Coalescing (08h) - Interrupt Vector Configuration (09h) - Write Atomicity (0Ah) - Asynchronous Event Configuration (0Bh) - Timestamp (0Eh) - LBA Status Information Report Interval(15h) - - Sanitize Config(17h) - Software Progress Marker (80h) - Host Identifier (81h) - NS Write Protection Config (84h)

0Ch	Asynchronous Event Request
0Dh	Namespace Management
10h	Firmware Commit
11h	Firmware Image Download
14h	Device Self-test
15h	Namespace Attachment
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize
85h - BFh	I/O Command Set Specific

6.1.1 Identify Command

The Identify Command returns the data described below.

[Table 150] Identify Controller Data Structure

Bytes	O/M	Default Value	Description
1:0	M	144Dh	PCI Vendor ID
3:2	M	144Dh	PCI Subsystem Vendor ID
23:4	M	SXXXNXXXXXXXXX	Serial Number (ASCII), X: Variables
63:24	M	1.9TB : SAMSUNG MZWLO15THBLA-00B5C 3.8TB : SAMSUNG MZWLO1T9HCJR-00B5C 7.6TB : SAMSUNG MZWLO3T8HCLS-00B5C 15.2TB : SAMSUNG MZWLO7T6HBLA-00B5C	Model Number (ASCII)
71:64	M	XXXXXXXQ	Firmware Revision, X: Variables
72	M	3h	Recommended Arbitration Burst
75:73	M	002538h	IEEE OUI Byte 73 - 38h Byte 74 - 25h Byte 75 - 0h
76	O	0h	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)
77	M	5h	Maximum Data Transfer Size(MDTS)
79:78	M	81h	Controller ID (CNTLID)
83:80	M	10400h	Version (VER)
87:84	M	1.92TB,3.84TB,7.68TB: 989680h 15.36TB: E4E1C0h	RTD3 Resume Latency (RTD3R)
91:88	M	1.92TB,3.84TB,7.68TB: 989680h 15.36TB: E4E1C0h	RTD3 Entry Latency (RTD3E)
95:92	M	300h	Optional Asynchronous Event Supported (OAES)
99:96	M	80h	Controller Attributes (CTRATT)
110:100		-	Reserved
111	M	1h	Controller Type
127:112	O	0h	FRU Globally Unique Identifier
129:128	O	0h	Command Retry Delay Time 1
131:130	O	0h	Command Retry Delay Time 2
133:132	O	0h	Command Retry Delay Time 3
239:134		-	Reserved
255:240	Refer to the NVMe Management Interface Specification for definition.		
257:256	M	5Fh	Optional Admin Command Support
258	M	7Fh	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)
259	M	Fh	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)
260	M	17h	Firmware Updates
261	M	1Eh	Log Page Attributes
262	M	FFh	Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)
263	M	0h	Number of Power States Support (0's based value)
264	M	1h	Admin Vendor Specific Command Configuration
265	O	0h	Autonomous Power State Transition Attributes (APSTA)
267:266	M	161h (80°C)	Warning Composite Temperature Threshold (WCTEMP)

269:268	M	168h (87°C)	Critical Composite Temperature Threshold (CCTEMP)
271:270	O	82h	Maximum Time for Firmware Activation (MTFA)
275:272	O	0h	Host Memory Buffer Preferred Size (HMPRE):
279:276	O	0h	Host Memory Buffer Minimum Size (HMMIN):
295:280	O	1.92TB : 1BF1FC56000h 3.84TB : 37E3EE56000h 7.68TB : 6FC7D256000h 15.36TB : DF880000000h	Total NVM Capacity (TNVMCAP):
311:296	O	0h	Unallocated NVM Capacity (UNVMCAP):
315:312	O	0h	Replay Protected Memory Block Support (RPMBS):
317:316	O	2h	Extended Device Self-test Time (EDSTT)
318	O	1h	Device Self-test Options (DSTO)
319	M	FFh	Firmware Update Granularity (FWUG)
321:320	M	0h	Keep Alive Support(KAS)
327:322	-	0h	Host Controlled Thermal Manageet
331:328	O	60000003h	Sanitize Capabilities (SANICAP)
335:332	O	0h	Host Memory Buffer Minimum Descriptor Entry Size
337:336	O	0h	Host Memory Maximum Descriptors Entries
339:338	O	0h	NVM Set Identifier Maximum
341:340	O	0h	Endurance Group Identifier Maximum
342	O	0h	ANA Transition Time
343	O	0h	Asymmetric Namespace Access Capabilities
347:344	O	0h	ANA Group Identifier Maximum
351:348	O	0h	Number of ANA Group Identifiers
355:352	O	50h	Persistent Event Log Size
511:332	-	-	Reserved
512	M	66h	Submission Queue Entry Size
513	M	44h	Completion Queue Entry Size
515:514	M	0h	Maximum Outstanding Commands
519:516	M	20h	Number of Namespaces
521:520	M	DFh	Optional NVM Command Support
523:522	M	0h	Fused Operation Support
524	M	4h	Format NVM Attributes
525	M	6h	Volatile Write Cache
527:526	M	FFFFh	Atomic Write Unit Normal All commands atomic
529:528	M	0h	Atomic Write Unit Power Fail (0's based value)
530	M	1h	NVM Vendor Specific Command Configuration
531	M	1h	Namespace Write Protection Capabilities
533:532	O	0h	Atomic Compare & Write Unit (ACWU)
535:534	M	-	Reserved
539:536	O	F0002h	SGL Support (SGLS)
767:540	M	-	Reserved
1023:768	M	nqn.1994-11.com.samsung:nvme:PM1743:2.5-inch:SXXXNXXXXXXXX	NVM Subsystem NVMe Qulified Name(SUBNQN)
I/O Command Set Attributes			
2047:1024	-	-	Reserved
Power State Descriptors			
2079:2048	M	-	Power State 0 Descriptor
2111:2080	O	-	Power State 1 Descriptor
2143:2112	O	-	Power State 2 Descriptor

2175:2144	O	-	Power State 3 Descriptor
2207:2176	O	-	Power State 4 Descriptor
…	-	-	
3071:3040	O	-	Power State 31 Descriptor (N/A)
4095:3072	-	0h	Samsung Reserved

[Table 151] Identify Power State Descriptor Data Structure

Bits	Default Value	Description
255:184	0	Reserved
183:182	2h	Active Power Scale(APS)
181:179	0	Reserved
178:176	2h	Active Power Workload(APW)
175:160	9C4h	Active Power(ACTP)
159:152	0	Reserved
151:150	2h	Idle Power Scale(IPS)
149:144	0	Reserved
143:128	384h	Idle Power(IDLP)
127:125	0	Reserved
124:120	0	Relative Write Latency
119:117	0	Reserved
116:112	0	Relative Write Throughput
111:109	0	Reserved
108:104	0	Relative Read Latency
103:101	0	Reserved
100:96	0	Relative Read Throughput
95:64	0h	Exit Latency (100us)
63:32	0h	Entry Latency (100us)
31:26	0h	Reserved
25	0h	Non-Operational State(NOPS)
24	0h	Max Power Scale(MXPS)
23:16	0h	Reserved
15:00	09C4h	Maximum Power

[Table 152] Identify Namespace Data Structure

Bytes	O/M	Default Value	Description
7:0	M	1.92TB : FD8FE2B0h 3.84TB : 1BF1F72B0h 7.68TB : 37E3E92B0h 15.36TB : 6FC400000h	Namespace Size
15:8	M	1.92TB : FD8FE2B0h 3.84TB : 1BF1F72B0h 7.68TB : 37E3E92B0h 15.36TB : 6FC400000h	Namespace Capacity
23:16	M	1.92TB : FD8FE2B0h 3.84TB : 1BF1F72B0h 7.68TB : 37E3E92B0h 15.36TB : 6FC400000h	Namespace Utilization
24	M	0h	Namespace Features Bits 7:1 Reserved Bit 0: Thin provisioning not supported
25	M	0h	Number of LBA Formats
26	M	10h	Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format
27	M	0h	Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA
28	M	0h	End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of Metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information
29	M	0h	End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bit 3 – 1: Protection information transferred as first 8 bytes of Metadata Bit 3 – 0: Protection information transferred as last 8 bytes of Metadata Bit 2:0 – 000b: Protection information disabled Bit 2:0 – 1h: Protection type 1 enabled Bit 2:0 – 2h: Protection type 2 enabled Bit 2:0 – 3h: Protection type 3 enabled
30	O	0h	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC):
31	O	0h	Reservation Capabilities (RESCAP):
32	O	80h	Format Progress Indicator (FPI)
33	O	9h	Deallocate Logical Block Features (DLFEAT):
35:34	O	0h	Namespace Atomic Write Unit Normal (NAWUN)
37:36	O	0h	Namespace Atomic Write Unit Power Fail (NAWUPF)
39:38	O	0h	Namespace Atomic Compare & Write Unit (NACWU)
41:40	O	0h	Namespace Atomic Boundary Size Normal (NABSN)
43:42	O	0h	Namespace Atomic Boundary Offset (NABO)
45:44	O	0h	Namespace Atomic Boundary Size Power Fail (NABSPF)
47:46	-	-	Reserved
63:48		1.92TB : 1BF1FC56000h 3.84TB : 37E3EE56000h 7.68TB : 6FC7D256000h 15.36TB : DF880000000h	NVM Capacity (NVMCAP)
103:64	-	-	Reserved
119:104	O	Device Dependant	Namespace Globally Unique Identifier (NGUID)
127:120	O	0h	IEEE Extended Unique Identifier(EUI64)
131:128	M	0090000h	LBA Format 0 Support

135:132	O	0h	LBA Format 1 Support
139:136	O	0h	LBA Format 2 Support
143:140	O	0h	LBA Format 3 Support
147:144	O	0h	LBA Format 4 Support
191:188	O	-	LBA Format 15 Support (N/A)
383:192	-	-	Reserved
Vendor Specific			
4095:384	-	-	Samsung Reserved

[Table 153] LBA Format 0 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	0h	Metadata Size

[Table 154] LBA Format 1 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	0h	LBA Data Size
15:00	MS	0h	Metadata Size

[Table 155] LBA Format 2 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	0h	LBA Data Size
15:00	MS	0h	Metadata Size

[Table 156] LBA Format 3 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	0h	LBA Data Size (2^n bytes)
15:00	MS	0h	Metadata Size (bytes)

[Table 157] LBA Format 4 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	0h	LBA Data Size (2^n bytes)
15:00	MS	0h	Metadata Size (bytes)

6.2 NVM Express I/O Command Set

[Table 158] Opcode for NVM Express I/O Commands

Opcode (Hex)	Command Name
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Write Zeroes
09h	Dataset Management
0Dh	Reservation Register
0Eh	Reservation Report
11h	Reservation Acquire
15h	Reservation Release

NOTE:
1) Deallocate feature in Dataset Management command is only supported in the Samsung SSD PM1743.

6.3 SMART/Health Information

[Table 159] SMART/Health Information Log

Bytes	Default Value	Attribute Description
0	0	Critical Warning Bit 7:5 – Reserved Bit 4 – 1h: the volatile memory backup device has failed. (only valid if the controller has a volatile memory backup solution) Bit 3 – 1h: the media has been placed in read only mode Bit 2 – 1h: the NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability Bit 1 – 1h: a temperature is above an over temperature threshold or below an under temperature threshold Bit 0 – 1h: the available spare space has fallen below the threshold
2:1	current temp.	Temperature
3	100	Available Spare
4	10	Available Spare Threshold
5	0	Percentage Used
31:6	-	Reserved
47:32	0	Data Units Read
63:48	0	Data Units Written
79:64	0	Host Read Commands
95:80	0	Host Write Commands
111:96	0	Controller Busy Time
127:112	0	Power Cycles
143:128	0	Power On Hours
159:144	0	Unsafe Shutdowns
175:160	0	Media and Data Integrity Errors
191:176	0	Number of Error Information Log Entries
195:192	0	Warning Composite Temperature Time
199:196	0	Critical Composite Temperature Time
201:200	current temp.	Temperature Sensor 1
203:202	Not support	Temperature Sensor 2
205:204	Not support	Temperature Sensor 3
207:206	Not support	Temperature Sensor 4
209:208	Not support	Temperature Sensor 5
211:210	Not support	Temperature Sensor 6
213:212	Not support	Temperature Sensor 7
215:213	Not support	Temperature Sensor 8
219:216	Not support	Thermal Management Temperature 1 Transition Count
223:220	Not support	Thermal Management Temperature 2 Transition Count
227:224	Not support	Total Time For Thermal Management Temperature 1
231:228	Not support	Total Time For Thermal Management Temperature 2
511:232	-	Reserved

7.0 NVMe-MI SMBus RESOURCES

This section listed data structures and registers accessible through SMBus interface.
Vital Product Data (VPD) is stored in SM-Bus slave address of 0xA6 (bits 7-1 correspond to 1010_011x on the SM-Bus).
H/W Temperature sensor SM-Bus slave address is 0x36 (bits 7-1 correspond to 0011_011x).
The legacy f/w simulated temperature sensor is located at SMBus slave address 0x38 (bits 7-1 correspond to 0011_100x).
The MI-Basic is accessible at 0xD4 (bits 7-1 correspond to 1101_010x).

7.1 Vital Product Data (VPD) Structure

VPD listed device specific information for Enterprise PCIe SSD discovery and power allocation.
* Data offset of VPD EEPROM is 1 Byte(8 bit).

Currently, VPD is provided following SFF U.2 format as following

[Table 160] Common Header

Byte Offset	Factory Default	Value	Description
0	01h	01h	**IPMI Format Version Number (IPMIVER):** This field indicates the IPMI Format Version.
1	Impl Spec	0h	**Internal Use Area Starting Offset (IUAOFF):** This field indicates the starting offset in multiples of 8 bytes for the Internal Use Area. A value of 00h may be used to indicate the Internal Use Area is not present.
2	Impl Spec	0h	**Chassis Info Area Starting Offset (CIAOFF):** This field indicates the starting offset in multiples of 8 bytes for the Chassis Info Area. A value of 00h may be used to indicate the Chassis Info Area is not present.
3	Impl Spec	0h	**Board Info Area Starting Offset (BIAOFF):** This field indicates the starting offset in multiples of 8 bytes for the Board Info Area. A value of 00h may be used to indicate the Board Info Area is not present.
4	01h	01h	**Product Info Area Starting Offset (PIAOFF):** This field indicates the starting offset in multiples of 8 bytes for the Product Info Area.
5	0Fh	0Fh	**MultiRecord Info Area Starting Offset (MRIOFF):** This field indicates the starting offset in multiples of 8 bytes for the MultiRecord Info Area.
6	00h	-	Reserved
7	Impl Spec	EFh	**Common Header Checksum (CHCHK):** Checksum computed over bytes 0 through 6. The checksum is computed by adding the 8-bit value of the bytes modulo 256 and then taking the 2's complement of this sum. When the checksum and the sum of the bytes module 256 are added, the result should be 0h.

[Table 161] Product Info Area (offset 8 bytes)

Byte Offset	Factory Default	Value	Description
0	01h	1h	**IPMI Format Version Number (IPMIVER)**: This field indicates the IPMI Format Version.
1	0Eh	Eh	**Product Info Area Length (PALEN)**: This field indicates the length of the product info area in multiples of 8 bytes. 112 bytes/8 = 14 = 0x0Eh
2	19h	19h	**Language Code (LCODE):** This field indicates the language used. A value of 19h is used to indicate English.
3	C8h	C8h	**Manufacturer Name Type/Length (MNTL):** This byte indicates the type and length of the Manufacturer Name field.
11:4	Impl Spec	Samsung	**Manufacturer Name (MNAME):** This field indicates the Manufacturer name in 8-bit ASCII. Unused bytes should be NULL characters.
12	D8h	D8h	**Product Name Type/Length (PNTL):** This byte indicates the type and length of the Product Name field.Product Name Type/Length (PNTL)
36:13	Impl Spec	PM1743	**Product Name (PNAME):** This field indicates the Product name in 8-bit ASCII. Unused bytes should be NULL characters. The PNAME value shall correspond to the Marketing Product Name (MP) FConfig tokenProduct Name (PNAME): This field indicates the Product name in 8-bit ASCII. Unused bytes should be NULL characters.
37	E8h	E8h	**Product Part/Model Number Type/Length (PPMNNTL):** This byte indicates the type and length of the Product Part/Model Number field.Product Part/Model Number Type/Length (PPMNNTL):
77:38	Impl Spec	PM1743	**Product Part/Model Number (PPMN)**: This field indicates the Product Part/Model Number in 8-bit ASCII. Unused bytes should be NULL characters.
78	C2h	C2h	**Product Version Type/Length (PVTL):** This byte indicates the type and length of the Product Part/Model Number field.
80:79	Impl Spec	1 (30h,31h)	**Product Version (PVER):** This field indicates the Product Version in 8-bit ASCII. Unused bytes should be NULL characters. Characters.
81	D4h	D4h	Product Serial Number Type/Length (PSNTL): This byte indicates the type and length of the Product Serial Number field.
101:82	Impl Spec	Vendor Unique	**Product Serial Number (PSN):** This field indicates the Product Serial Number in 8-bit ASCII. Unused bytes should be NULL characters. This field should contain the same value as the Serial Number (SN) field in the NVMe Identify Controller Data Structure.
102	0h	00h	**Asset Tag Type/Length (ATTL):** This byte indicates the type and length of the Asset Tag field. A value of 00h may be used to indicate an Asset Tag is not present.
103	0h	00h	**FRU File ID Type/Length (FFTL):** This byte indicates the type and length of the FRU File ID field. A value of 00h may be used to indicate a FRU File ID is not present.
104	C1h	C1h	**End of Record (EOR)**: A value of C1h in this byte indicates the end of recordEnd of Record (EOR):
110:105	-	-	Reserved
111	Impl Spec	FCh	**Product Info Area (PICHK):** Checksum computed over bytes 0 through 110. The checksum is computed by adding the 8-bit value of the byes modulo 256 and then taking the 2's complement of this sum. When the checksum and the sum of the bytes module 256 are added, the result should be 0h.

[Table 162] NVMe MultiRecord Area

Byte Offset	Factory Default	Value	Description
0	0Bh	0Bh	NVMe Record Type ID
1	2h	02h	Bit 7 – end of list; record format version = 2h
2	28h	3Bh	**Record Length (RLEN)**: This field indicates the length of the MultiRecord Area in bytes.
3	Impl Spec	ACh	**Record Checksum**: This field is used to give the record data a zero checksum (i.e., the modulo 256 sum of the record data bytes from byte offset 05 through the end of this record plus this checksum byte equals zero.
4	Impl Spec	0Ch	**Header Checksum**: This field is used to give the record header data a zero checksum (i.e., the modulo 256 sum of the record header data bytes from byte offset 05 through the end of this record plus this checksum byte equals zero.
5	0h	0h	**NVMe MultiRecord Area Version Number:** This field indicates the version number of this multirecord. This field shall be set to 0h in this version of the specification.
6	Impl Spec	0x13 (19) (2.5" Form Factor - (SFF-TA-1001) 15mm)	**Management Endpoint Form Factor (MEFF):** This field indicates the form factor of the Management Endpoint.
12:7	-	-	Reserved
13	Impl Spec	0h	**Initial 1.8V Power Supply Requirements:** This field specifies the initial 1.8V power supply requirements in Watts prior to receiving a Set Slot Power message.
14	Impl Spec	0h	**Maximum 1.8V Power Supply Requirements:** This field specifies the maximum 1.8V power supply requirements in Watts. A value of zero indicates that the power supply voltage is not used.Maximum.
15	Impl Spec	0h	**Initial 3.3V Power Supply Requirements**: This field specifies the initial 3.3V power supply requirements in Watts prior to receiving a Set Slot Power message.
16	Impl Spec	0h	**Maximum 3.3V Power Supply Requirements**: This field specifies the maximum 3.3V power supply requirements in Watts. A value of zero indicates that the power supply voltage is not used.
17	-	-	Reserved
18	Impl Spec	2h	**Maximum 3.3V aux Power Supply Requirements:** This field specifies the maximum 3.3V power supply requirements in 10 mW units. A value of zero indicates that the power supply voltage is not used.
19	Impl Spec	0h	**Initial 5V Power Supply Requirements**: This field specifies the initial 5V power supply requirements in Watts prior to receiving a Set Slot Power message.
20	Impl Spec	0h	**Maximum 5V Power Supply Requirements**: This field specifies the maximum 5V power supply requirements in Watts. A value of zero indicates that the power supply voltage is not used.
21	Impl Spec	9h	**Initial 12V Power Supply Requirements:** This field specifies the initial 12V power supply requirements in Watts prior to receiving a Set Slot Power message.
22	Impl Spec	19h	**Maximum 12V Power Supply Requirements**: This field specifies the maximum 12V power supply requirements in Watts. A value of zero indicates that the power supply voltage is not used.
23	Impl Spec	19h	**Maximum Thermal Load**: This field specifies the maximum thermal load from the NVM Subsystem in Watts.
36:24	Impl Spec	1.92TB: 1BF1FC56000h 3.84TB: 37E3EE56000h 7.68TB: 6FC7D256000h 15.3TB: DF880000000h	**Total NVM Capacity:** This field indicates the total NVM capcity of the Management Endpoint in bytes. If the NVM Subsystem supports Namespace Management, then this field should correspond to the value reported in the TNVMCAP field in the NVMe Identify Controller Data structure. A value of 0h may be used to indicate this feature is not supported.
63:37	-	-	Reserved

[Table 163] NVMe PCIe Port MultiRecord Area

Byte Offset	Factory Default	Value	Description
0	0Ch	Ch	NVMe PCIe Port Record Type ID
1	2h	82h	Bit 7 – end of list; record format version = 2h
2	28h	Bh	**Record Length (RLEN)**: This field indicates the length of the MultiRecord Area in bytes.
3	Impl Spec	D3h	**Record Checksum**: This field is used to give the record data a zero checksum (i.e., the modulo 256 sum of the record data bytes from byte offset 05 through the end of this record plus this checksum byte equals zero)
4	Impl Spec	94h	**Header Checksum**: This field is used to give the record header a zero checksum (i.e., the modulo 256 sum of the preceding record bytes starting with the first byte of the header plus this checksum byte equals zero.
5	0h	0h	**NVMe PCIe Port MultiRecord Area Version Number:** This field indicates the version number of this multirecord. This field shall be set to zero in this version of the specification.
6	Impl Spec	0h	**PCIe Port Number:** This field contains the PCIe port number. This is the same value as that reported in the Port Number field in the PCIe Link Capabilities Register.
7	Impl Spec	1h	**Port Information:** This field indicates information about the PCIe Ports in the device. Bits [7:1] Reserved Bit [0] Bit 0, if set to '1' indicates that all PCIe ports within the device have the same capabilities (i.e., the capabilities listed in this structure are consistent across each PCIe port).
8	Impl Spec	1Fh	**PCIe Link Speed:** This field indicates a bit vector of link speeds supported by the PCIe port.PCIe Link Speed**:** This field indicates a bit vector of link speeds supported by the PCIe port.
9	Impl Spec	4h	**PCIe Maximum Link Width:** The maximum PCIe link width for this NVM Subsystem port. This is the expected negotiated link width that the port link trains to if the platform supports it. A Management Controller may compare this value with the PCIe Negotiated Link Width to determine if there has been a PCIe link training issue.
10	Impl Spec	1h	MCTP Support**:** This field contains a bit vector that specifies the level of support for the NVMe Management Interface.
11	Impl Spec	8h	**Ref Clk Capability:** This field contains a bit vector that specifies the PCIe clocking modes supported by the port. Bits [7:4] Reserved Bit [3] Set to '1' if the device automatically uses RefClk if provided and otehrwise uses SRIS Bit [2] Set to '1' if the PCIe link supports Separate ReClk with SSC (SRIS) Bit [1] Set to '1' if the PCIe link supports Separate ReClk with no SSC (SRNS). Bit [0] Set to '1' if the PCIe link supports common ReClk.
15:12	0h	-	Reserved

8.0 PRODUCT COMPLIANCE

8.1 Product Regulatory Compliance and Certifications

Category	Certifications
Safety	cUL
	CE
	TUV-GS
	CB
EMC	CE (EU)
	BSMI (Taiwan)
	KC (South Korea)
	VCCI (Japan)
	RCM (Australia)
	FCC (USA) / IC (Canada)

The three existing compliance marks (C-Tick, A-Tick, and RCM) are consolidated into a single compliance mark - the RCM.

Caution: Any changes or modifications in construction of this device which are not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE:
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications, However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio / TV technician for help.
Modifications not expressly approved by the manufacturer could void the user's authority to operated the equipment under FCC rules.

1. 기자재 명칭 : SSD (Solid State Drive)
2. 모델명(Model): 라벨 별도 표기
3. 제조연월 : 라벨 별도 표기
4. 제조자 : 삼성전자(주)
5. 제조국가 : 대한민국
6. 상호명 : 삼성전자(주)

Industry Canada ICES-003 Compliance Label:
CAN ICES-3 (B)/NMB-3(B)

9.0 REFERENCES

[Table 164] Standards References

Item	Website
PCI Express® Base Specification Revision 5.0	http://pcisig.com/specifications
NVM Express™ Specification Rev. 1.4	http://www.nvmexpress.org/
Enterprise SSD Form Factor Version 1.0a	http://www.ssdformfactor.org/
Solid-State Drive Requirements and Endurance Test Method (JESD218B)	https://www.jedec.org/standards-documents/docs/jesd218B01
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a