SAMSUNG SSD 845DC PRO

Data Sheet, Ver. 1.0

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Revision History

Revision No.	History	Date
Ver.1.0	Initial Release	June 2014

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1. General Description

Samsung SSD 845DC PRO is designed for server and data centers. 845DC PRO's superior performance and industry-leading reliability are suitable for the most demanding data center uses. Especially, 845DC PRO's significantly enhanced endurance through 3D V-NAND technology and reinforced random write performance will provide the best optimized solution for write-intensive applications with heavier workloads.

845DC PRO			
Capacity	400GB, 800GB		
Application	Mixed and write-intensive usages are recommended		
Dimensions (LxWxH)	(100.20±0.25) x (69.85±0.25) x (6.80±0.20) mm		
Weight	Max. 65g (800GB)		
Interface	Serial ATA 6Gb/s (compatible with SATA 3Gb/s and SATA 1.5Gb/s) Fully complies with ATA/ATAPI-7 Standard(Partially Complies with ATA/ATAPI-8) Support NCQ : Up to 32 depth		
Form Factor	2.5" type		
Controller	Samsung 3-core MDX controller		
NAND Flash Memory	Samsung 3D V-NAND 2bit MLC		
DRAM Cache memory	512MB (400GB), 1GB (800GB)		
Performance*	Sequential Read:	Up to. 530 MB/s	
	Sequential Write:	Up to. 460 MB/s	
	Random Read (4KB, QD32):	Max. 92,000 IOPS	
	Random Write (4KB, QD32):	Max. 50,000 IOPS (400GB) Max. 51,000 IOPS (800GB)	
Quality of Service (4KB, QD32)	99.99%	Read: 0.6ms	Write: 5ms
	Max.	Read: 3ms	Write: 12ms
Latency (4KB, QD1)	Sequential	Read :45 us	Write : 40us
	Random	Read :110us	Write : 50us
Reliability	- Mean Time Between Failures (MTBF) : 2,000,000 hours - Uncorrectable Bit Error Rate (UBER) : 1 sector per 10^{17} bits read - End-to-end data protection		
TBW	10 Drive Writes per Day (DWPD)		
Power Consumption	Active (Read / Write) : 1.7 Watt / 3.1Watt(400GB), 3.3Watt(800GB) Idle : 1.0 Watt		
Temperature	Operating:	0°C to 70°C	
	Non-Operating:	-40°C to 85°C	
Humidity	5% to 95%, non-condensing		
Vibration	Non-Operating:	20~2000Hz, 20G	
Shock	Non-Operating:	1500G , duration 0.5m sec, 3 axis	
Certification	CE, BSMI, KCC, VCCI, C-tick, FCC, IC, UL, TUV, CB		
RoHS compliance	ROHS2		
Warranty	5 years limited		

* Actual performance may vary depending on use conditions and environment

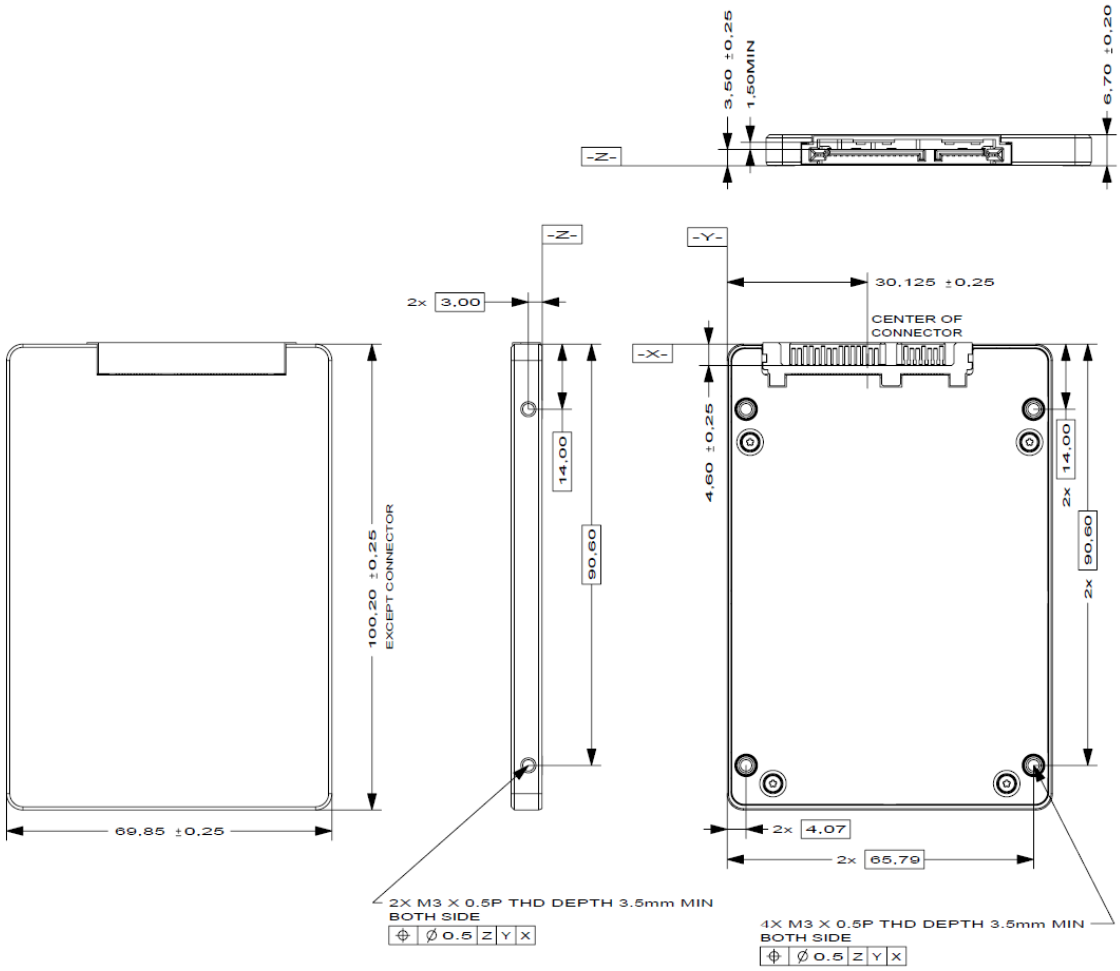
1. Performance measured using FIO with queue depth 32
2. Measurements are performed on whole LBA range
3. Write cache enabled
4. 1MB/sec = 1,048,576 bytes/sec was used in sequential performance
5. Uncorrectable Bit Error Rate (UBER) and Endurance (TBW) is based on JEDEC standard.

2. Mechanical Specification

2.1 Physical dimensions and Weight

Model Name	Height	Width	Length	Weight
MZ-7WD400 MZ-7WD800	6.80±0.20	69.85±0.25	100.20±0.25	Max. 65g

※ For the thickness size(height), drive label thickness was included



[Figure 2-1] Physical dimension

3. Product Specifications

3.1 Interface and Configuration

Burst read/write rate is 600 MB/sec (6Gb/s).
Fully compatible with ATA-7 Standard
(Partially Complies with ATA/ATAPI-8)

3.2 Capacity

	MZ-7WD400	MZ-7WD800
Unformatted Capacity	400 GB	800 GB
User-addressable Capacity (Number of sectors)	781,422,768	1,562,824,368
Byte per Sector	512 Bytes	

※ 1 Megabyte (MB) = 1 Million bytes; 1 Gigabyte (GB) = 1 Billion bytes
Actual usable capacity may be less due to formatting, partitioning, operating system, application and otherwise.

3.3 Performance

3.3.1 Sequential Read/Write Bandwidth

Sequential (128KB, MB/s)	Model Name	
	MZ-7WD400	MZ-7WD800
Read	530	530
Write	460	460

3.3.2 Random Read/Write Input/Output Operations Per Second (IOPS)

4KB Random (IOPS)		MZ-7WD400	MZ-7WD800
QD 32	Read IOPS	92,000	92,000
	Write IOPS	50,000	51,000
QD 1	Read IOPS	8,500	8,500
	Write IOPS	18,000	18,000

8KB Random (IOPS)		MZ-7WD400	MZ-7WD800
QD 32	Read IOPS	59,000	59,000
	Write IOPS	25,000	25,000
QD 1	Read IOPS	7,500	7,500
	Write IOPS	16,000	16,000

※ Actual performance may vary depending on usage conditions and system environment.
1. Performance measured FIO with queue depth 32
2. Measurements are performed on whole LBA range
3. Write cache enabled
4. 1MB/sec = 1,048,576 bytes/sec was used in sequential performance

3.3.3 IOPS Consistency

4KB		MZ-7WD400	MZ-7WD800
Random Read (%)	QD1	98	99
	QD32	99	98
Random Write (%)	QD1	96	97
	QD32	95	95

8KB		MZ-7WD400	MZ-7WD800
Random Read (%)	QD1	98	99
	QD32	99	99
Random Write (%)	QD1	96	96
	QD32	95	95

※ IOPS Consistency [%] = (99.9% IOPS)/(Average IOPS) x 100

3.3.4 Latency

		MZ-7WD400	MZ-7WD800
Read (us)	Typical 4KB Random	110	110
	Typical Sequential	45	45
Write (us)	Typical 4KB Random	50	50
	Typical Sequential	40	40

※ Latency is measured using 4KB transfer size with Queue Depth 1.

3.3.5 Quality of Service (QoS)

Quality of Service (QoS) is the level of quality that provides steady and consistent performance given as a maximum response time under the certain confidence level of 99.9% or 99.9999%.

QD1		MZ-7WD400		MZ-7WD800	
		Read	Write	Read	Write
99.9% (ms)	4KB	0.2	0.2	0.2	0.2
	8KB	0.2	0.3	0.2	0.3
Max (99.9999%) (ms)	4KB	1.0	5.0	1.0	5.0
	8KB	1.0	7.0	1.0	7.0

QD32		MZ-7WD400		MZ-7WD800	
		Read	Write	Read	Write
99.9% (ms)	4KB	0.6	5.0	0.6	5.0
	8KB	1.0	7.0	1.0	7.0
Max (99.9999%) (ms)	4KB	3.0	12.0	3.0	12.0
	8KB	3.0	15.0	3.0	15.0

※ Actual performance may vary depending on usage conditions and system environment.
Test condition: Intel® i3-3240 3.40GHz, 4GB DDR3-1600, Intel C216 Family Chipset
RedHat Enterprise Linux 6.4 with AHCI (ver.9.3.0.1011)
Test program: FIO 2.1.3

3.4 Electrical Characteristics

3.4.1 Supply Voltage

Characteristics	Requirements
Allowable voltage	5V ± 5%
Allowable noise/ripple	100mV p-p or less
Rise time (Max./Min.)	1s / 1ms
Fall time	500ms
Inrush current (Typical Peak)	1.5A, <1s

※ The 845DC PRO needs only 5V power rail, and the 12V power pin of a SATA connector is not connected to any net and components in the 845DC PRO.
If both 12V and 5V power rails are provided to the SSD, the SSD would work well.
If only 5V power rail is provided to the SSD, the SSD would work well.
If only 12V power rail is provided to the SSD, the SSD would not work, but this won't bring any problems to host system.

3.4.2 Power Consumption

		MZ-7WD400	MZ-7WD800
Active Read (Watt)	Average	1.7	1.7
	Burst	2.6	2.8
Active Write (Watt)	Average	3.1	3.3
	Burst	4.8	5.1
Idle (Watt)		1.0	1.0

3.4.3 Power Loss Protection (PLP)

Samsung 845DC PRO SSD is built with tantalum capacitors to protect all data in the write cache in case of a power failure. On detection of the external power loss, the SSD uses the electricity from a tantalum capacitor to transfer the cached data in DRAM to the flash memory.
This enterprise-grade PLP provides an added level of security to ensure that valuable write information is well protected against data corruption caused by sudden power loss.

	MZ-7WD400	MZ-7WD800
Number of Capacitors	15	18
Capacitance	1.5mF	1.8mF
Discharging time	Min 35ms	

3.5 Reliability

	MZ-7WD400	MZ-7WD800
Mean Time Between Failures (MTBF)	2,000,0000 Hours	
Uncorrectable Bit Error Rate (UBER)	1 sector per 10^17 bits read	
Endurance(TBW)	10 Drive Writes per Day (DWPD)	
Data Retention	3 months (@40℃)	
Power on/off cycle	24 per Day	
Insertion cycle	500 cycles	

※ Refer to JESD218 standard table 1 for requirements of enterprise SSD reliability.

3.6 Environmental Specifications

Features	Operating	Non-Operating
Temperature	0℃ to 70℃	-40℃ to 85℃
Humidity	5% to 95%, non-condensing	
Vibration	1~2KHz, 20Grms, 20min/3-axis	
Shock	1500G with 0.5ms duration	

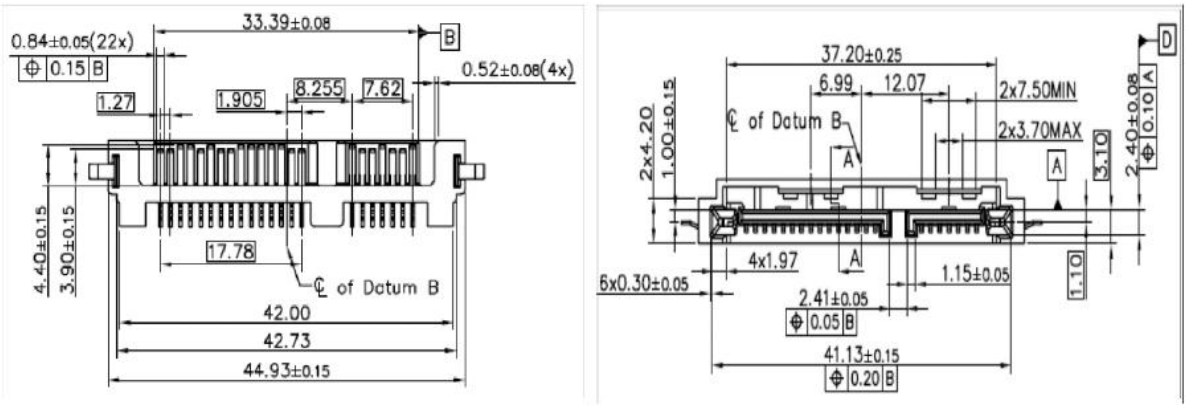
※ Notes :

1. Temperature specification is following JEDEC standard; Expressed temperature must be measured right on the case.
2. Humidity is measured in non-condensing.
3. Shock test condition: 0.5ms duration with half sine wave.
4. Vibration test condition: 10Hz to 2,000Hz, 15mins/axis on 3axis(X,Y,Z)

4. Electrical Interface Specification

4.1 Serial ATA Interface connector

Drive Connector : AMPHENOL, SATA-001-0009-1-TR



4.2 Pin Assignments

	No.	Plug Connector pin definition	
Signal	S1	GND	2nd mate
	S2	A+	Differential signal A from Phy
	S3	A-	
	S4	GND	2nd mate
	S5	B-	Differential signal A from Phy
	S6	B+	
	S7	GND	2nd mate
Key and spacing separate signal and power segments			
Power	P1	V33	3.3V power (Unused)
	P2	V33	3.3V power (Unused)
	P3	V33	3.3V power, pre-charge, 2nd mate (Unused)
	P4	GND	1st mate
	P5	GND	2nd mate
	P6	GND	2nd mate
	P7	V5	5V power, pre-charge, 2nd mate
	P8	V5	5V power
	P9	V5	5V power
	P10	GND	2nd mate
	P11	DAS/DSS	Device Activity Signal/Disable Staggered Spinup
	P12	GND	1st mate
	P13	V12	12V power, pre-charge, 2nd mate (Unused)
	P14	V12	12V power (Unused)
	P15	V12	12V power (Unused)

5. Shadow Register Block registers Description

5.1 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. All other registers required for the command must be set up before writing the Command Register.

5.2 Device Control Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. All other registers required for the command must be set up before writing the Command Register

5.2.1 Field/bit description

7	6	5	4	3	2	1	0
HOB	-	-	-	-	SRST	nIEN	0

※ HOB is defined by the 48bit Address feature set. A write to any Command register shall clear the HOB bit to zero.

※ SRST is the host software reset bit. SRST=1 indicates that the drive is held reset and sets BSY bit in Status register. Setting SRST=0 re-enables the device.

※ nIEN is the enable bit for the device Assertion of INTRQ to the host. When nIEN=0, and the device is selected by Drive select bit in DEVICE/HEAD register, device interrupt to the host is enabled. When this bit is set, the "I' bit in the Register Host to Device, PIO setup, Set Device Bits and DMA Set Up will be set, whether pending interrupt is found or not.

5.3 Device / Head Register

5.3.1 Field / bit description

The content of this register shall take effect when written.

7	6	5	4	3	2	1	0
-	L	-	DEV	HS3	HS2	HS1	HS0

※ L : Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.

※ DEV: Device select. Cleared to zero selects Device 0. Set to one selects Device1.

※ HS3, HS2, HS1, HS0 : Head select bits. The HS3 through HS0 contain bits 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.

5.4 Error Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. All other registers required for the command must be set up before writing the Command Register.

5.4.1 Field / bit description

7	6	5	4	3	2	1	0
ICRC	UNC	0	IDNF	0	ABRT	TKONF	AMNF

※ ICRC: Interface CRC Error. CRC=1 indicates a CRC error has occurred on the data bus during a Ultra-DMA transfer.

※ UNC: Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.

※ IDNF: ID Not Found. IDN=1 indicates the requested sector's ID field could not be found .

※ ABRT: Aborted Command. ABT=1 indicates the requested command has been aborted due to a device status error or an invalid parameter in an output register.

※ TKONF: Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.

※ AMNF: Address Mark Not Found. When AMN=1, it indicates that the data address mark has not been found after finding the correct ID field for the requested sector.

5.5 Features Register

This register is command specific. This is used with the Set Features command, S.M.A.R.T. Function Set command.

5.6 Cylinder High (LBA High)

This register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.

5.7 Cylinder Low (LBA Mid) Register

This register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15. When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 8-15, and the "previous content" contains Bits 32-39

5.8 Sector Number (LBA low) Register

This register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7. When 48-bit commands are used, the "most recently written" content contains LBA Bits 0-7, and the "previous content" contains Bits 24-31.

5.9 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors (in 28-bit addressing) or 65,536 sectors (in 48-bit addressing) is specified. If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request. The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

5.10 Status Register

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command. If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read. If BSY=1, no other bits in the register are valid. And read/write operations of any other register are negated in order to avoid the returning of the contents of this register instead of the other registers' contents.

5.10.1 Field / bit description.

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

※ BSY : Busy. BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.

※ DRDY : Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to 0 during power on until the device is ready to accept a command.

※ DF : Device Fault. DF=1 indicates that the device has detected a write fault condition. DF is set to 0 after the Status Register is read by the host.

※ DSC : Device Seek Complete. DSC=1 indicates that a seek has completed and the device head is settled over a track. DSC is set to 0 by the device just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current seek complete status. When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of not spinning up.

※ DRQ : Data Request. DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.

※ CORR : Corrected Data. Always 0.

※ IDX : Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX for timing purposes.

※ ERR : ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets

6. Command Descriptions

6.1 Supported ATA Commands

Command Name	Command Code(Hex)	Command Name	Command Code(Hex)
CHECK POWER MODE	E5h	STANDBY	E2h
DATA SET MANAGEMENT	06h	STANDBY IMMEDIATE	E0h
DEVICE CONFIGURATION FREEZE LOCK	B1/C1	WRITE BUFFER	E8h
DEVICE CONFIGURATION IDENTIFY	B1/C2	WRITE BUFFER DMA	EBh
DEVICE CONFIGURATION RESTORE	B1/C0	WRITE DMA	CAh
DEVICE CONFIGURATION SET	B1/C3	WRITE DMA EXT	35h
DOWNLOAD MICROCODE	92h	WRITE DMA FUA EXT	3Dh
DOWNLOAD MICROCODE DMA	93h	WRITE DMA WITHOUT RETRY	CBh
EXECUTE DEVICE DIAGNOSTIC	90h	WRITE FPDMA QUEUED	61h
FLUSH CACHE	E7h	WRITE LOG DMA EXT	57h
FLUSH CACHE EXT	EAh	WRITE LOG EXT	3Fh
IDENTIFY DEVICE	ECh	WRITE MULTIPLE	C5h
IDLE	E3h	WRITE MULTIPLE EXT	39h
IDLE IMMEDIATE	E1h	WRITE MULTIPLE FUA EXT	CEh
INITIALIZE DEVICE PARAMETERS	91h	WRITE SECTORS	30h
NOP	00h	WRITE SECTORS EXT	34h
READ BUFFER	E4h	WRITE SECTORS WITHOUT RETRY	31h
READ BUFFER DMA	E9h	WRITE UNCORRECTABLE EXT	45h
READ DMA	C8h		
READ DMA EXT	25h		
READ DMA WITHOUT RETRIES	C9h		
READ FPDMA QUEUED	60h		
READ LOG DMA EXT	47h		
READ LOG EXT	2Fh		
READ MULTIPLE	C4h		
READ MULTIPLE EXT	29h		
READ NATIVE MAX ADDRESS	F8h		
READ NATIVE MAX ADDRESS EXT	27h		
READ SECTORS	20h		
READ SECTORS EXT	24h		
READ SECTORS WITHOUT RETRY	21h		
READ VERIFY SECTORS	40h		
READ VERIFY SECTORS EXT	42h		
READ VERIFY SECTORS WITHOUT RETRY	41h		
RECALIBRATE	10h		
RECEIVE FPDMA QUEUED	65h		
SECURITY DISABLE PASSWORD	F6h		
SECURITY ERASE PREPARE	F3h		
SECURITY ERASE UNIT	F4h		
SECURITY FREEZE LOCK	F5h		
SECURITY SET PASSWORD	F1h		
SECURITY UNLOCK	F2h		
SEEK	70h		
SEND FPDMA QUEUED	64h		
SET MAX ADDRESS	F9h		
SET MAX ADDRESS EXT	37h		
SET MULTIPLE MODE	C6h		
SLEEP	E6h		
SMART	B0h		

6.2 SECURITY FEATURE Set

The Security mode features allow the host to implement a security password system to prevent unauthorized access to the disk drive.

6.2.1 SECURITY mode default setting

The SSD is shipped with master password set to 00h value(ASCII blanks) and the lock function disabled. The system manufacturer/dealer may set a new master password by using the SECURITY SET PASSWORD command, without enabling the lock function.

6.2.2 Initial setting of the user password

When a user password is set, the drive automatically enters lock mode by the next powered-on.

6.2.3 SECURITY mode operation from power-on

In locked mode, the SSD rejects media access commands until a SECURITY UNLOCK command is successfully completed.

6.2.4 Password lost

If the user password is lost and High level security is set, the drive does not allow the user to access any data. However, the drive can be unlocked using the master password. If the user password is lost and Maximum security level is set, it is impossible to access data. However, the drive can be unlocked using the ERASE UNIT command with the master password. The drive will erase all user data and unlock the drive.

6.3 SMART FEATURE Set (B0h)

The SMART Feature Set command provides access to the Attribute Values, the Attribute Thresholds, and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The SMART Feature Set command has several separate subcommands which are selectable via the device's Features Register when the SMART Feature Set command is issued by the host. In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Feature Set command.

6.3.1 Sub Command

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

Command Name	Code	Command Name	Code
SMART READ DATA	D0h	SMART WRITE LOG	D6h
SMART READ ATTRIBUTE THRESHOLDS	D1h	SMART ENABLE OPERATIONS	D8h
SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	D2h	SMART DISABLE OPERATIONS	D9h
SMART SAVE ATTRIBUTE VALUES	D3h	SMART RETURN STATUS	DAh
SMART EXECUTE OFF-LINE IMMIDIATE	D4h	SMART ENABLE/DISABLE AUTOMATIC OFF-LINE	DBh
SMART READ LOG	D5h		

6.3.1.1 S.M.A.R.T. Read Attribute Values (subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the S.M.A.R.T. Read Attribute Values subcommand from the host, the device asserts BSY, saves any updated attribute Values to the Attribute Data sectors, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Value information from the device via the Data Register.

6.3.1.2 S.M.A.R.T. Read Attribute Thresholds (subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the S.M.A.R.T. Read Attribute Thresholds subcommand from the host, the device reads the Attribute Thresholds from the Attribute Threshold sectors and then waits for the host to transfer the 512 bytes of Attribute Thresholds information from the device

6.3.1.3 S.M.A.R.T. Enable/Disable Attribute Auto-save (subcommand D2h)

This subcommand enables and disables the attribute auto save feature of the device. The S.M.A.R.T. Enable/Disable Attribute Auto-save subcommand allows the device to automatically save its

updated Attribute Values to the Attribute Data Sector at the timing of the first transition to Active idle mode and after 15 minutes after the last saving of Attribute Values. This subcommand causes the auto save feature to be disabled. The state of the Attribute Auto-save feature—either enabled or disabled—will be preserved by the device across the power cycle. A value of 00h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Auto-save subcommand— will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or a power-down. A value of F1h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Auto-save subcommand— will cause this feature to be enabled. Any other nonzero value written by the host into this register before issuing the S.M.A.R.T. Enable/Disable Attribute Auto-save subcommand will not change the current Auto-save status. The device will respond with the error code specified in Table: "S.M.A.R.T. Error Codes" on page 26. The S.M.A.R.T. Disable Operations subcommand disables the auto save feature along with the device's S.M.A.R.T. operations. Upon the receipt of the subcommand from the host, the device asserts BSY, enables or disables the Auto-save feature, clears BSY, and asserts INTRQ.

6.3.1.4 S.M.A.R.T. Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Auto-save feature. Upon receipt of the S.M.A.R.T. Save Attribute Values subcommand from the host, the device asserts BSY, writes any updated Attribute Values to the Attribute Data sector, clears BSY, and asserts INTRQ.

6.3.1.5 S.M.A.R.T. Execute Off-line Immediate (subcommand D4h)

This subcommand causes the device to immediately initiate the set of activities that collect Attribute data in an offline mode (off-line routine) or execute a self-test routine in either captive or off-line mode. The LBA Low register shall be set to specify the operation to be executed

LBA Low	Subcommand
00h	Execute S.M.A.R.T. off-line data collection routine immediately
01h	Execute S.M.A.R.T. Short self-test routine immediately in off-line mode
02h	Execute S.M.A.R.T. Extended self-test routine immediately in off-line mode
03h	Reserved
04h	Execute S.M.A.R.T. Selective self-test routine immediately in off-line mode
40h	Reserved
7Fh	Abort off-line mode self-test routine
81h	Execute S.M.A.R.T. short self-test routine immediately in captive mode
82h	Execute S.M.A.R.T. Extended self-test routine immediately in captive mode
84h	Execute S.M.A.R.T. selective self-test routine immediately in captive mode
C0h	Reserved

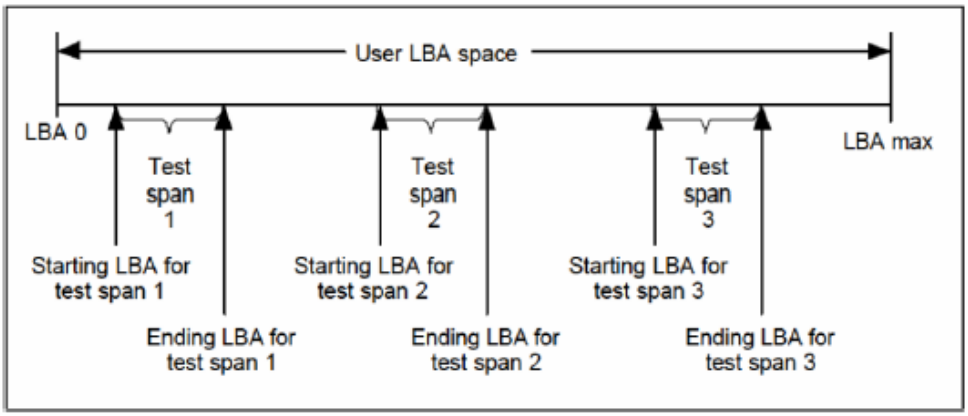
Off-line mode : The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.
Captive mode : When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte (see Table "Device Attribute Data Structure" on page 6.3.2) and ATA registers and then executes the command completion. See definitions below.

Status Set ERR to one when the self-test
Error Set ABRT to one when the self-test
LBA Low Set to F4h when the self-test has failed
LBA High Set to 2Ch when self-test has failed

6.3.1.6 S.M.A.R.T. Selective self-test routine

When the value in the LBA Low register is 4 or 132, the Selective self-test routine shall be performed. This self test routine shall include the initial tests per-formed by the Extended self-test routine plus a selectable read scan. The host shall not write the Selective self-test log while the execution of a Selective self-test command is in progress. The user may choose to do read scan

only on specific areas of the media. To do this, user shall set the test spans desired in the Selective self-test log and set the flags in the Feature flags field of the Selective self-test log to indicate do not perform off-line scan. In this case, the test spans defined shall be read scanned in their entirety. The Selective self-test log is updated as the self-test proceeds indicating test progress. When all specified test spans have been completed, the test is terminated and the appropriate self-test execution status is reported in the SMART READ DATA response depending on the occurrence of errors. Below figure shows an example of a Selective self test definition with three test spans defined. In this example, the test terminates when all three test spans have been scanned.



After the scan of the selected spans described above, a user may wish to have the rest of media read scanned as an off-line scan. In this case, the user shall set the flag to enable off-line scan in addition to the other settings. If an error occurs during the scanning of the test spans, the error is reported in the self-test execution status in the SMART READ DATA response and the off-line scan is not executed. When the test spans defined have been scanned, the device shall then set the offline scan pending and active flags in the Selective self-test log to one, the span under test to a value greater than five, the self-test execution status in the SMART READ DATA response to 00h, set a value of 03h in the off-line data collection status in the SMART READ DATA response and shall proceed to do an off-line read scan through all areas not included in the test spans. This off-line read scan shall completed as rapidly as possible, no pauses between block reads, and any errors encountered shall not be reported to the host. Instead error locations may be logged for future reallocation. If the device is powered-down before the off-line scan is completed, the off-line scan shall resume when the device is again powered up. From power-up, the resumption of the scan shall be delayed the time indicated in the Selective self-test pending time field in the Selective self-test log. During this delay time the pending flag shall be set to one and the active flag shall be set to zero in the Selective self-test log. Once the time expires, the active flag shall be set to one, and the off-line scan shall resume. When the entire media has been scanned, the off-line scan shall terminate, both the pending and active flags shall be cleared to zero, and the off-line data collection status in the SMART READ DATA response shall be set to 02h indicating completion. During execution of the Selective self-test, the self-test executions time byte in the Device SMART Data Structure may be updated but the accuracy may not be exact because of the nature of the test span segments. For this reason, the time to complete off-line testing and the self-test polling times are not valid. Progress through the test spans is indicated in the selective self-test log. A hardware or software reset shall abort the Selective self-test except when the pending bit is set to one in the Selective self-test log). The receipt of a SMART EXECUTE OFF-LINE IMMEDIATE command with 0Fh, Abort off-line test routine, in the LBA Low register shall abort Selective self-test regardless of where the device is in the execution of the command. If a second self-test is issued while a selective self-test is in progress, the selective self-test is aborted and the newly requested self-test is executed.

6.3.1.7 S.M.A.R.T. Read Log Sector (subcommand D5h)

This command returns the indicated log sector contents to the host. Sector count specifies the number of sectors to be read from the specified log. The log transferred by the drive shall start at the first sector in the specified log, regardless of the sector count requested. Sector number indicates the log sector to be returned as described in the following Table.

LBA Low	Subcommand	
00h	Log directory	RO
01h	SMART error log	RO
02h	Comprehensive SMART error log	RO
04h-05h	Reserved	RO
06h	SMART self-test log	RO
08h	Reserved	RO
09h	Selective self-test log	R/W
0Ah-7Fh	Reserved	RO
80h-9Fh	Host vendor specific	R/W
A0h-FFh	Reserved	VS

RO – Log is read only by the host.
R/W – Log is read or written by host.
VS - Log is vendor specific thus read/write ability is vendor specific.

6.3.1.8 S.M.A.R.T. Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector. The 512 bytes of data are transferred at a command and the LBA Low value shall be set to one. The LBA Low shall be set to specify the log sector address. If a Rea Only log sector is specified, the device returns ABRT error.

6.3.1.9 S.M.A.R.T. Enable Operations (subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of a S.M.A.R.T. Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T.—either enabled or disabled—will be preserved by the device across power cycles. Once enabled, the receipt of subsequent S.M.A.R.T. Enable Operations subcommands will not affect any of the Attribute Values. Upon receipt of the S.M.A.R.T. Enable Operations subcommand from the host, the device asserts BSY, enables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

6.3.1.10 S.M.A.R.T. Disable Operations (subcommand D9h)

This subcommand disables all S.M.A.R.T. capabilities within the device including the device's attribute auto save feature. After receipt of this subcommand the device disables all S.M.A.R.T. operations. Non self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T.—either enabled or disabled—is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute auto saving. Upon receipt of the S.M.A.R.T. Disable Operations subcommand from the host, the device asserts BSY, disables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ. After receipt of the device of the S.M.A.R.T. Disable Operations subcommand from the host, all other S.M.A.R.T. subcommands—with the exception of S.M.A.R.T. Enable Operations—are disabled, and invalid and will be aborted by the device—including the S.M.A.R.T. Disable Operations subcommand— returning the error code as specified in Table: “S.M.A.R.T. Error Codes” on page 6.3.8. Error reporting. Any Attribute Values accumulated and saved to volatile memory prior to receipt of the S.M.A.R.T. Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a S.M.A.R.T. Read Attribute Values or a S.M.A.R.T. Save Attribute Values command

6.3.1.11 S.M.A.R.T. Return Status (subcommand DAh)

This subcommand is used to communicate the reliability status of the device to the host's request. Upon receipt of the S.M.A.R.T. Return Status subcommand the device asserts BSY, saves any updated Attribute Values to the reserved sector, and compares the updated Attribute Values to the Attribute Thresholds. If the device does not detect a Threshold Exceeded Condition, or detects a Threshold Exceeded Condition but involving attributes are advisory, the device loads 4Fh into the LBA Mid register, C2h into the LBA High register, clears BSY, and asserts INTRQ. If the device detects a Threshold Exceeded Condition for pre-failure attributes, the device loads F4h into the

LBA Mid register, 2Ch into the LBA High register, clears BSY, and asserts INTRQ. Advisory attributes never result in a negative reliability condition.

6.3.1.12 S.M.A.R.T. Enable/Disable Automatic Off-line (subcommand DBh)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that cause the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities. The Sector Count register shall be set to specify the feature to be enabled or disabled:

Sector Count	Feature Description
00h	Disable Automatic Off-line
F8h	Enable Automatic Off-line

A value of zero written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic off-line data collection feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation such as during a power-on, during a power-off sequence, or during an error recovery sequence. A value of F8h written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic Off-line data collection feature to be enabled. Any other non-zero value written by the host into this register before issuing this subcommand is vendor specific and will not change the current Automatic Off-Line Data Collection and Off-line Read Scanning status. However, the device may respond with the error code specified in Table: “S.M.A.R.T. Error Codes” on 6.3.8 Error reporting.

6.3.2 Device Attribute Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Values subcommand.

Device Attribute Data Structure

Byte	Description
0 ~ 1	Data structure revision number
2 ~ 361	1st - 30th Individual attribute data
362	Off-line data collection status
363	Self-test execution status
364 ~ 365	Total time in seconds to complete off-line data collection activity
366	Vendor Specific
367	Off-line data collection capability
368 ~ 369	SMART capability
370	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	Self-test failure check point
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374 ~ 510	Reserved
511	Data structure checksum

6.3.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number will be set to 0005h. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

6.3.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Byte	Description
0	Attribute ID number 01-FFh
1 ~ 2	Status flag bit 0 (pre-failure/advisory bit) bit 0 = 0: If attribute value is less than the threshold, the drive is in advisory condition. Product life period may be expired. bit 0 = 1: If attribute value is less than the threshold, the drive is in pre-failure condition. The drive may have failure. bit 1 (on-line data collection bit) bit 1 = 0: Attribute value will be changed during off-line data collection operation. bit 1 = 1: Attribute value will be changed during normal operation. bit 2 (Performance Attribute bit) bit 3 (Error rate Attribute bit) bit 4 (Event Count Attribute bit) bit 5 (Self-Preserving Attribute bit) bit 6-15 Reserved
3	Attribute value 01h-FDh *1 00h, FEh, FFh = Not in use 01h = Minimum value 64h = Initial value Fdh = Maximum value
4	Worst Ever normalized Attribute Value (valid values from 01h-FEh)
5 ~ 10	Raw Attribute Value Attribute specific raw data (FFFFFFh - reserved as saturated value)
11	Reserved(00h)
*1 For ID = 199 CRC Error Count	

Attribute ID Numbers: Any nonzero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers.

ID	Attribute name
5	**Reallocated Sector Count**
9	**Power-on Hours**
12	**Power-on Count**
177	**Wear Leveling Count**
179	**Used Reserved Block Count (total)**
180	**Unused Reserved Block Count (total)**
181	**Program Fail Count (total)**
182	**Erase Fail Count (total)**
183	**Runtime Bad Count (total)**
184	**End to End Error data path Error Count**
187	**Uncorrectable Error Count**
190	**Air Flow Temperature**
195	**ECC Error Rate**
199	**CRC Error Count**
202	**SSD Mode Status**
235	**Power Recovery Count**
241	**Total LBA Written**
242	**Total LBA Read**
250	**SATA Interface Downshifts (total)**

6.3.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates an Automatic Off-line Data Collection Status.

Bit 7	Automatic Off-line Data Collection Status
0	Automatic Off-line Data Collection is disabled.
1	Automatic Off-line Data Collection is enabled.

Bits 0–6 represent a hexadecimal status value reported by the device

Value	Definition
0	Off-line data collection never started.
2	All segments completed without errors. In this case the current segment pointer is equal to the total segments required.
3	Off-line activity in progress.
4	Off-line data collection is suspended by the interrupting command.
5	Off-line data collecting is aborted by the interrupting command.
6	Off-line data collection is aborted with a fatal error.

6.3.2.4 Self-test execution status

Bit	Definition	
0-3	Percent Self-test remaining. An approximation of the percent of the self-test routine remaining until completion given in ten percent increments. Valid values are 0 through 9.	
4-7	Current Self-test execution status.	
	0	The self-test routine completed without error or has never been run.
	1	The self-test routine was aborted by the host.
	2	The self-test routine was interrupted by the host with a hard or soft reset.
	3	The device was unable to complete the self-test routine due to a fatal error or unknown test error.
	4	The self-test routine was completed with an unknown element failure.
	5	The self-test routine was completed with an electrical element failure.
	6	The self-test routine was completed with a servo element failure.
	7	The self-test routine was completed with a read element failure.
	15	The self-test routine is in progress.

6.3.2.5 Total time in seconds to complete off-line data collection activity

This field tells the host how many seconds the device requires to complete the off-line data collection activity.

6.3.2.6 Current segment pointer

This byte is a counter indicating the next segment to execute as an off-line data collection activity. Because the number of segments is 1, 01h is always returned in this field

6.3.2.7 Off-line data collection capability

Bit	Definition	
0	Execute Off-line Immediate implemented bit	
	0	S.M.A.R.T. Execute Off-line Immediate subcommand is not implemented
	1	S.M.A.R.T. Execute Off-line Immediate subcommand is implemented
1	Enable/disable Automatic Off-line implemented bit	
	0	S.M.A.R.T. Enable/disable Automatic Off-line subcommand is not implemented
	1	S.M.A.R.T. Enable/disable Automatic Off-line subcommand is implemented
2	Abort/restart off-line by host bit	
	0	The device will suspend off-line data collection activity after an interrupting command and resume it after a vendor specific event
	1	The device will abort off-line data collection activity upon receipt of a new command Bit Definition
3	Off-line Read Scanning implemented bit	
	0	The device does not support Off-line Read Scanning
	1	The device supports Off-line Read Scanning
4	Self-test implemented bit	
	0	Self-test routing is not implemented
	1	Self-test routine is implemented
5	Reserved (0)	
6	Selective self-test routine is not implemented	
	0	Selective self-test routine is not implemented
	1	Selective self-test routine is implemented
7	Reserved (0)	

6.3.2.8 S.M.A.R.T. Capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the S.M.A.R.T. ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit	Definition
0	Pre-power mode attribute saving capability. If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).
1	Attribute auto save capability. If bit = 1, the device supports the S.M.A.R.T. ENABLE/ DISABLE ATTRIBUTE AUTOSAVE command.
2-15	Reserved (0)

6.3.2.9 Error logging capability

Bit	Definition
7-1	Reserved (0)
0	The Error Logging support bit. If bit = 1, the device supports the Error Logging

6.3.2.10 Self-test failure check point

This byte indicates the section of self-test where the device detected a failure.

6.3.2.11 Self-test completion time

These bytes are the minimum time in minutes to complete the self-test.

6.3.2.12 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

6.3.3 Device Attribute Thresholds data structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Thresholds. All multibyte fields shown in these data structures follow the ATA/ATAPI-6 specification for byte ordering, that is, that the least significant byte occupies the lowest numbered byte address location in the field. The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values

Device Attribute Thresholds Data Structure

Byte	Description
0 ~ 1	Data structure revision number
2 ~ 361	1st - 30th Individual attribute data
362 ~ 379	Reserved
380 ~ 510	Vendor Specific
511	Data structure checksum

6.3.3.1 Data Structure Revision Number

This value is the same as the value used in the Device Attributes Values Data Structure.

6.3.3.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure are in the same order and correspond to the entries in the Individual Attribute Data Structure.

Byte	Description
0	Attribute ID Number (01h to FFh)
1	Attribute Threshold (for comparison with Attribute Values from 00h to FFh) 00h - "always passing" threshold value to be used for code test purposes 01h - minimum value for normal operation FDh - maximum value for normal operation FEh - invalid for threshold value FFh - "always failing" threshold value to be used for code test purposes
2~11	Reserved (00h)

6.3.3.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

6.3.3.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable. However, the host might use the "S.M.A.R.T. Write Attribute Threshold" subcommand to override these preset values in the Threshold sectors.

6.3.3.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

6.3.4 S.M.A.R.T. Log Directory

The following defines the 512 bytes that make up the S.M.A.R.T. Log Directory. The S.M.A.R.T. Log Directory is on S.M.A.R.T. Log Address zero and is defined as one sector long.

S.M.A.R.T Log Directory

Byte	Description
0 ~ 1	S.M.A.R.T. Logging Version
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved
.....	
510	Number of sectors in the log at log address 255
511	Reserved

The value of the S.M.A.R.T. Logging Version word shall be 01h. The logs at log addresses 80-9Fh are defined as 16 sectors long.

6.3.5 S.M.A.R.T. error log sector

The following defines the 512 bytes that make up the S.M.A.R.T. error log sector. All multi-byte fields shown in these data structures follow the ATA/ATAPI- 6 specifications for byte ordering.

S.M.A.R.T error log sector

Byte	Description
0	S.M.A.R.T. error log version
1	Error log pointer
2 ~ 91	1st error log data structure
92 ~ 181	2nd error log data structure
182 ~ 271	3rd error log data structure
272 ~ 361	4th error log data structure
362 ~ 451	5th error log data structure
452 ~ 453	Device error count
454 ~ 510	Reserved
511	Data structure checksum

6.3.5.1 S.M.A.R.T. error log version

This value is set to 01h.

6.3.5.2 Error log pointer

This value points to the most recent error log data structure. Only values 1 through 5 are valid.

6.3.5.3 Device error count

This field contains the total number of errors. The value will not roll over.

6.3.5.4 Error log data structure

The data format of each error log structure is shown below.

Error log data structure

Byte	Description
n ~ n + 11	1st command data structure
n + 12 ~ n + 23	2nd command data structure
n + 24 ~ n +35	3rd command data structure
n+36 ~ n + 47	4th command data structure
n+48 ~ n + 59	5th command data structure
n+60 ~ n+89	Error data structure

6.3.5.5 Command data structure

Data format of each command data structure is shown below.

Command data structure

Byte	Description
n	Content of the Device Control register when the Command register was written
n+1	Content of the Features Control register when the Command register was written
n+2	Content of the Sector Count Control register when the Command register was written
n+3	Content of the LBA Low register when the Command register was written
n+4	Content of the LBA Mid register when the Command register was written
n+5	Content of the LBA High register when the Command register was written
n+6	Content of the Device/Head register when the Command register was written
n+7	Content written to the Command register
n+8	Timestamp
n+9	Timestamp
n+10	Timestamp
n+11	Timestamp

Timestamp shall be the time since power-on in milliseconds when command acceptance occurred. This timestamp may wrap around.

6.3.5.6 Error data structure

Data format of error data structure is shown below.

Error data structure

Byte	Description
n	Reserved
n+1	Content written to the Error register after command completion occurred.
n+2	Content written to the Sector Count register after command completion occurred.
n+3	Content written to the LBA Low register after command completion occurred.
n+4	Content written to the LBA Mid register after command completion occurred.
n+5	Content written to the LBA High register after command completion occurred.
n+6	Content written to the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 ~ n + 26	Extended error information
n+27	State
n+28	Life Timestamp (least significant byte)
n+29	Life Timestamp (most significant byte)

Extended error information is vendor specific which is not available for 845DC PRO

State field contains a value indicating the device state when command is issued to the device.

Byte	Description
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h ~ xAh	Reserved
xBh ~ xFh	Vendor unique

Vendor unique is not available for 845DC PRO.

6.3.6 Self-test log structure

The following defines the 512 bytes that make up a Self-test log sector.

Self-test log data structure

Byte	Description
0~1	Data structure revision
n*24 + 2	Self-test number
n*24 + 3	Self-test execution status
n*24 + 4 ~ n*24 + 5	Life timestamp
n*24 + 6	Self-test failure check point
n*24 + 7 ~ n*24 + 10	LBA of first failure
n*24 +11 ~ n*24 + 25	Vendor specific
.....	
506 ~ 507	Vendor specific
508	Self-test log pointer
509 ~ 510	Reserved
511	Data structure checksum

NOTE : N is 0 through 20

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

6.3.7 Selective self-test log data structure

The Selective self-test log is a log that may be both written and read by the host. This log allows the host to select the parameters for the self-test and to monitor the progress of the self-test. The following table defines the contents of the Selective self-test log which is 512 bytes long. All multi-byte fields shown in these data structures follow the specifications for byte ordering.

Byte	Description	Read/Write
0 – 1	Data structure revision	R/W
2 – 9	Starting LBA for test span 1	R/W
10 – 11	Ending LBA for test span 1	R/W
18 – 25	Starting LBA for test span 2	R/W
26 – 33	Ending LBA for test span 2	R/W
34 – 41	Starting LBA for test span 3	R/W
42 – 49	Ending LBA for test span 3	R/W
50 – 57	Starting LBA for test span 4	R/W
58 – 65	Ending LBA for test span 4	R/W
66 – 73	Starting LBA for test span 5	R/W
74 – 81	Ending LBA for test span 5	R/W
82 – 337	Reserved	Reserved
338 – 491	Vendor specific	Vendor Specific
492 – 499	Current LBA under test	Read
500 – 501	Current span under test	Read
502 – 503	Feature flags	R/W
504 – 507	Vendor Specific	Vendor Specific
508 – 509	Selective self-test pending time	R/W
510	Reserved	Reserved
511	Data structure checksum	R/W

6.3.8 Error reporting

The following table shows the values returned from the Status and Error Registers when specific error conditions are encountered by a device.

S.M.A.R.T Error Codes

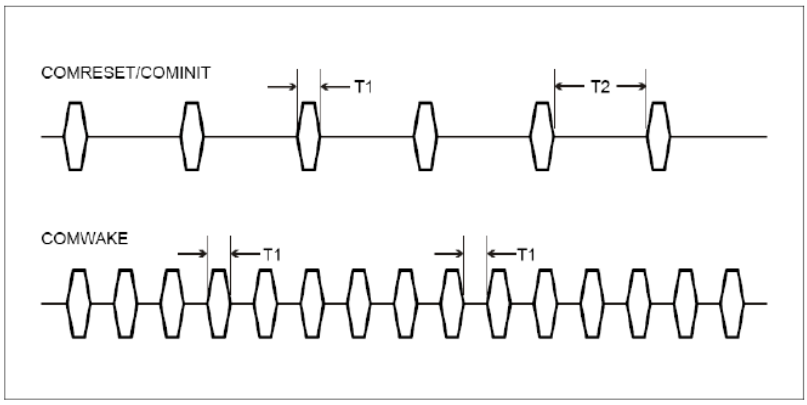
Error condition	Status Register	Error Register
A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the LBA High and LBA Mid registers.	51h	04h
A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A S.M.A.R.T. FUNCTION SET command subcommand other than S.M.A.R.T. ENABLE OPERATIONS was received by the device while the device was in a "S.M.A.R.T Disabled" state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure	51h	10h or 04h
The device is unable to write to its Attribute Values data structure.	51h	10h or 04h

7. OOB signaling and Phy Power State

7.1 OOB signaling

7.1.1 OOB signal spacing

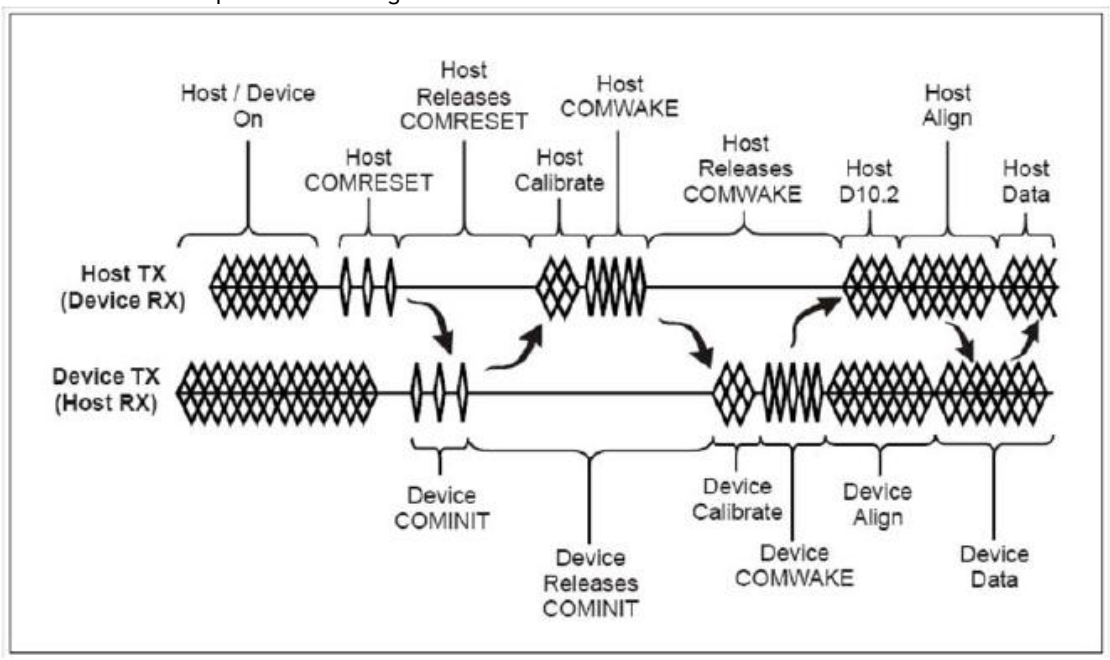
There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in following Figure and Table. The COMWAKE OOB signaling is used to bring the Phy out of a power-down state (Partial or Slumber)



Time	Value
T1	106.7 ns
T2	320ns

7.2 Phy Power State

7.2.1 COMRESET sequence state diagram



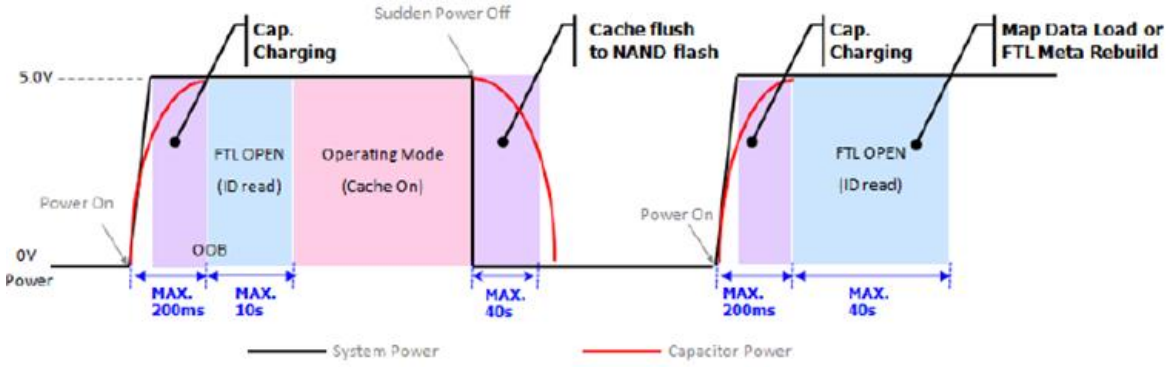
8. SPOR Specification (Sudden Power Off and Recovery)

8.1 Data Recovery in Sudden Power Off

If power interruption is detected, SSD dumps all cached user data and meta data to NAND Flash. SSD could protect even the user data in DRAM from sudden power off while SSD is used with cache on. Commonly, data is protected all of the operation period.

8.2 Time to Ready Sequence

In normal power-off recovery status, SSD needs less than 11 seconds to reach operating mode where SSD works perfectly with cache-on state. SSD is ready to respond Identify Device command during FTL OPEN. When the sudden power-off occurs, the user data in DRAM will be dumped into to NAND Flash using the stored power in the capacitor. In sudden power-off recovery condition, mapping data will be loaded or the FTL meta data be rebuilt perfectly for initial max. 40 seconds. During this period, Identify Device command is still supported. It is called SPOR.(Sudden Power Off and Recovery)



9. SATA II Optional Feature

9.1 Asynchronous Signal Recovery

Phys may support asynchronous signal recovery for those applications where the usage model of device insertion into a receptacle does not apply. When signal is lost, both the host and the device may attempt to recover the signal. A host or device shall determine loss of signal as represented by a transition from PHYRDY to PHYRDYn, which is associated with entry into states LSI: NoCommErr or LS2:NoComm within the Link layer. Note that negation of PHYRDY does not always constitute a loss of signal. Recovery of the signal is associated with exit from state LS2:NoComm. If the device attempts to recover the signal before the host by issuing a COMINIT, the device shall return its signature following completion of the OOB sequence which included COMINIT. If a host supports asynchronous signal recovery, when the host receives an unsolicited COMINIT, the host shall issue a COMRESET to the device. When a COMRESET is sent to the device in response to an unsolicited COMINIT, the host shall set the Status register to 7Fh and shall set all other Shadow Command Block Registers to FFh. When the COMINIT is received in response to the COMRESET which is associated with entry into state HP2B:HR_AwaitNoCOMINIT, the Shadow Status register value shall be updated to either FFh or 80h to reflect that a device is attached.

9.2 Power Segment Pin P11

Pin P11 of the power segment of the device connector may be used by the device to provide the host with an activity indication and it may be used by the host to indicate whether staggered spinup should be used. To accomplish both of these goals, pin P11 acts as an input from the host to the device prior to PHYRDY for staggered spin-up control and then acts as an output from the device to the host after PHYRDY for activity indication. The activity indication provided by pin P11 is primarily for use in backplane applications. A host may only support one pin P11 feature, either receiving activity indication or staggered spin-up disable control. If a host supports receiving activity indication via pin P11, then the host shall not use pin P11 to disable staggered spin-up. If a host does not support receiving activity indication via pin P11, then the host may use pin P11 to disable staggered spin-up.

9.3 Activity LED indications

The signal provides for activity indication. This is a low-voltage and low-current driver intended for efficient integration into present and future IC manufacturing processes. The signal is NOT suitable for directly driving an LED and must first be buffered using a circuit external to the drive before driving and LED. The LED indication signal is working on 200msec periods on FORMAT and Write same command. (100ms at high state and then 100msec at low state) On the other case of commands, the signal is working on 100msec periods.

10. Product Compliance

10.1 Product regulatory compliance and Certifications

Category	Certification
CE	Comunaute Europeenne
BSMI	Bureau of Standards, Metrology and Inspection
KCC	Korea Communications commission
VCCI	Voluntary Control Council for Interference
C-Tick	Radio Telecommunication Labeling
FCC	Federal Communications Commission
IC	Industry Canada
UL	Underwriters Laboratories, Inc.
TUV	Technischer Uberwachungs Vereine e.V
CB	Scheme of the IECEE for Mutual Recognition of Test Certificates for Electrical Equipment

Caution: Any changes or modifications in construction of this device which are not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE :

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications, However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment under FCC rules.

1. 기자재 명칭 : SSD (Solid State Drive)
2. 모델명(Model): 라벨 별도 표기
3. 제조연월 : 라벨 별도 표기
4. 제조자 : 삼성전자(주)
5. 제조국가 : 대한민국
6. 상호명 : 삼성전자(주)

Industry Canada ICES-003 Compliance Label:
CAN ICES-3 (B)/NMB-3(B)

11. Identify Device Data

Word	400GB	800GB	Description
0	0040h	0040h	General information
1	3FFFh	3FFFh	Obsolete
2	C837h	C837h	Specific configuration
3	0010h	0010h	Obsolete
4 – 5	0000h	0000h	Retired
6	003Fh	003Fh	Obsolete
7 – 8	0000h	0000h	Reserved for the Compact Flash Association
9	0000h	0000h	Retired
10 – 19	XXXXh	XXXXh	Serial Number (ATA string)
20 – 21	0000h	0000h	Retired
22	0000h	0000h	Obsolete
23 – 26	XXXXh	XXXXh	Firmware revision (ATA string)
27 – 46	XXXXh	XXXXh	Model number
47	8010h	8010h	Read/Write Multiple Support
48	4000h	4000h	Trusted Computing feature set options
49	2F00h	2F00h	Capabilities
50	4000h	4000h	Capabilities
51-52	0200h	0200h	Obsolete
53	0007h	0007h	Field Validity
54-58	3FFFh	3FFFh	Obsolete
59	D110h	D110h	Multiple Logical Setting
60	FFFFh	FFFFh	Total number of user addressable logical sectors for 28-bit commands
61	0FFFh	0FFFh	Total number of user addressable logical sectors for 28-bit commands
62	0000h	0000h	Obsolete
63	0007h	0007h	Multi-word DMA transfer
64	0003h	0003h	PIO transfer modes supported
65	0078h	0078h	Minimum Multiword DMA transfer cycle time per word (ns)
66	0078h	0078h	Manufacturer's recommended Multiword DMA cycle time (ns)
67	0078h	0078h	Minimum PIO transfer cycle time without IORDY flow control (ns)
68	0078h	0078h	Minimum PIO transfer cycle time with IORDY flow control (ns)
69	4F20h	4F20h	Additional supported
70 – 74	0000h	0000h	Reserved
75	001Fh	001Fh	Queue depth
76	850Eh	850Eh	Serial ATA capabilities
77	0046h	0046h	Reserved for Serial ATA
78	0064h	0064h	Serial ATA features supported
79	0064h	0064h	Serial ATA features enabled
80	03FCh	03FCh	Major version number
81	0039h	0039h	Minor version number
82	746Bh	746Bh	Commands and feature sets supported
83	7D01h	7D01h	Commands and feature sets supported
84	4163h	4163h	Commands and feature sets supported
85	7469h	7469h	Commands and feature sets supported or enabled
86	BC01h	BC01h	Commands and feature sets supported or enabled
87	4163h	4163h	Commands and feature sets supported or enabled
88	207Fh	207Fh	Ultra DMA Modes
89	0010h	0010h	Normal Security Erase Unit Time
90	0010h	0010h	Enhanced Security Erase Unit Time
91	0000h	0000h	Advanced Power Management Level
92	FFFEh	FFFEh	Master Password Revision Code
93	0000h	0000h	Hardware reset result

Word	400GB	800GB	Description
94	0000h	0000h	Obsolete
95	0000h	0000h	Stream Minimum Request Size
96	0000h	0000h	Streaming Transfer Time - DMA
97	0000h	0000h	Streaming Access Latency - DMA and PIO
98 – 99	0000h	0000h	Streaming Performance Granularity (DWord)
100 – 103	XXXXh	XXXXh	Total Number of User 48-Bit LBA
104	0000h	0000h	Streaming Transfer Time - PIO
105	0008h	0008h	Maximum number of 512-byte data blocks of LBA Range Entries per DATA SET MANAGEMENT command
106	4000h	4000h	Physical sector size / logical sector size
107	0000h	0000h	Inter-seek delay for ISO 7779 standard acoustic testing 108 5002h
108	5002h	5002h	World wide name
109	5388h	5388h	World wide name
110 – 111	XXXXh	XXXXh	World wide name
112 – 115	0000h	0000h	Reserved
116	0000h	0000h	Reserved
117 – 118	0000h	0000h	Logical sector size (Dword)
119	401Eh	401Eh	Commands and feature sets supported
120	401Ch	401Ch	Commands and feature sets supported or enabled
121 – 126	0000h	0000h	Reserved for expanded supported and enabled settings
127	0000h	0000h	Obsolete
128	0029h	0029h	Security status
129 – 159	0000h	0000h	Vendor specific
160	0000h	0000h	CFA power mode
161 – 167	0000h	0000h	Reserved for the CFA(Compact Flash Association)
168	0000h	0000h	Device Nominal Form Factor
169	0001h	0001h	DATA SET MANAGEMENT is supported
170 – 173	2020h	2020h	Additional Product Identifier (ATA string)
174 – 175	0000h	0000h	Reserved
176 – 205	0000h	0000h	Current Media Serial Number
206	003Dh	003Dh	SCT Command Transport
207 – 208	0000h	0000h	Reserved
209	4000h	4000h	Alignment of logical blocks within a physical block
210 – 211	0000h	0000h	Write-Read-Verify Sector Count Mode 3
212 – 213	0000h	0000h	Write-Read-Verify Sector Count Mode 2
214	0000h	0000h	Obsolete
215 – 216	0000h	0000h	Obsolete
217	0001h	0001h	Nominal media rotation rate
218	0000h	0000h	Reserved
219	0000h	0000h	Obsolete
220	0000h	0000h	Write Read Verify Mode
221	0000h	0000h	Reserved
222	107Fh	107Fh	Transport major version number
223	0000h	0000h	Transport major version number
224 – 229	0000h	0000h	Reserved
230 – 233	0000h	0000h	Extended Number of User Addressable Sectors
234	0000h	0000h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
235	0800h	0800h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
236 - 242	0000h	0000h	Reserved
243	0000h	0000h	FDE_function
244-254	0000h	0000h	Reserved
255	0AA5h	0AA5h	Integrity Word

12. Product line up

Density	Model Name	Model Code	Box Contents
400 GB	MZ-7WD400	MZ-7WD400EW	Basic (SSD, warranty, Label)
800 GB	MZ-7WD800	MZ-7WD800EW	Basic (SSD, warranty, Label)
400 GB	MZ-7WD400	MZ-7WD400Z	Bulk (SSD)
800 GB	MZ-7WD800	MZ-7WD800Z	Bulk (SSD)

For more information, please visit www.samsung.com/ssd.
To download the latest software & manuals, please visit www.samsung.com/samsungssd.